

Revision: 1.0

TITLE

TITLE

[illegible]

GIGABYTE™			
Title COVER SHEET			
Size B	Document Number N650SLI-DS4L	Rev 1.0	
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Version: 1.0

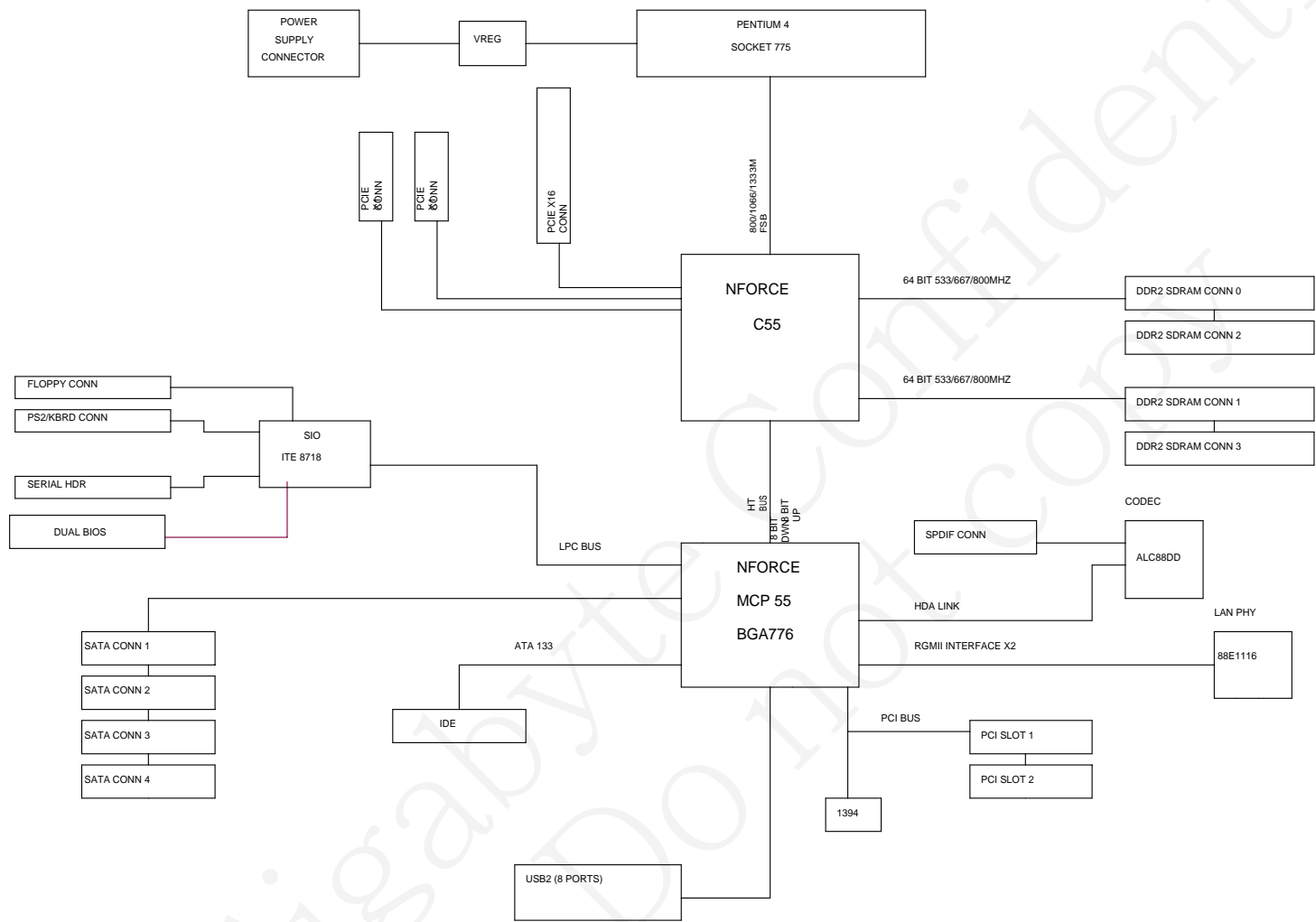
Component value change history

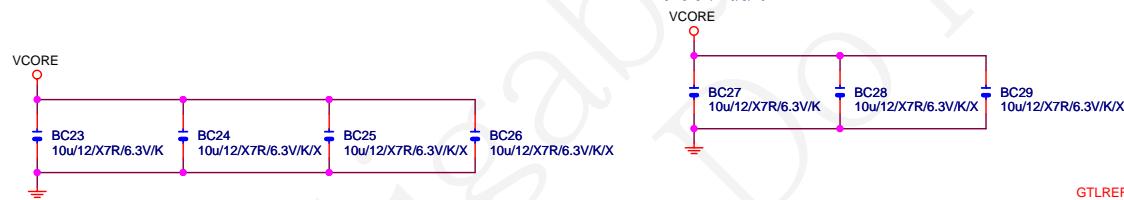
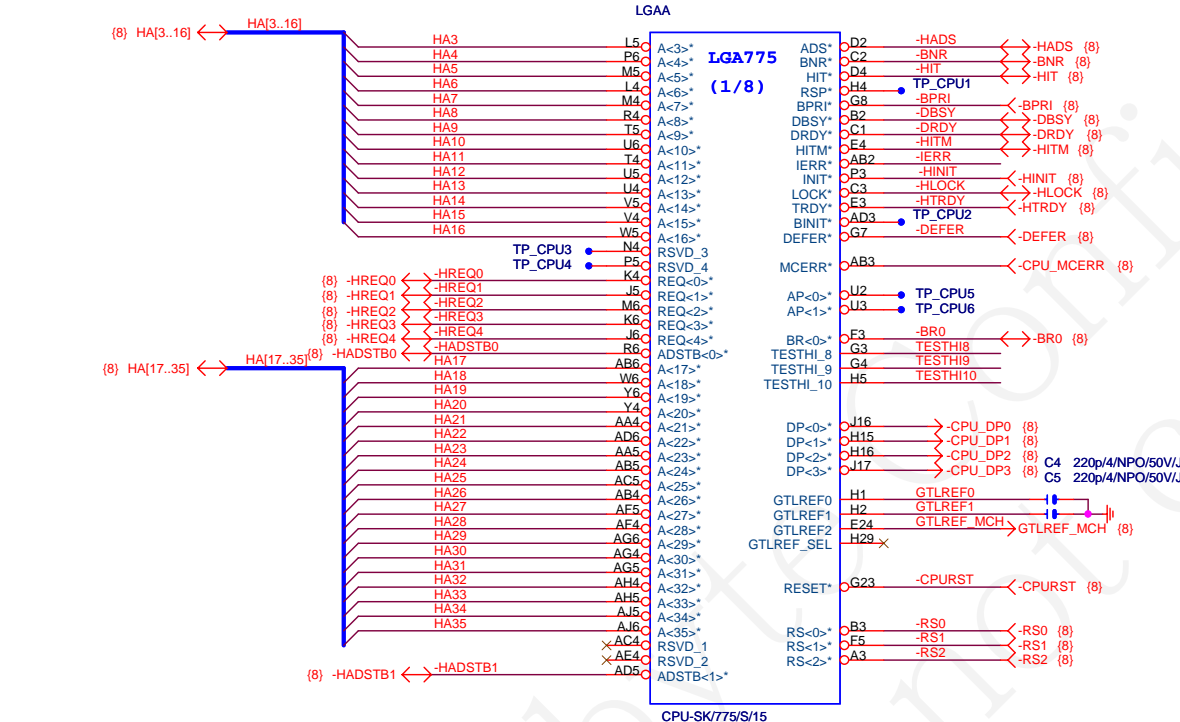
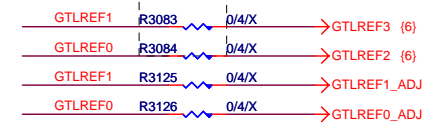
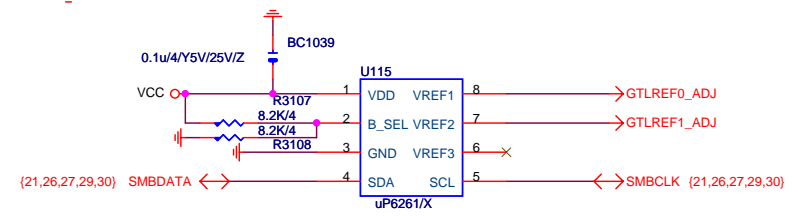
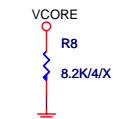
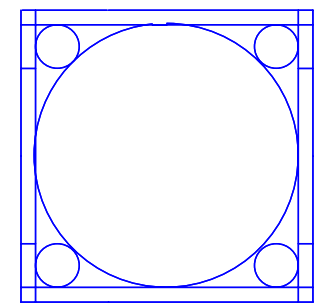
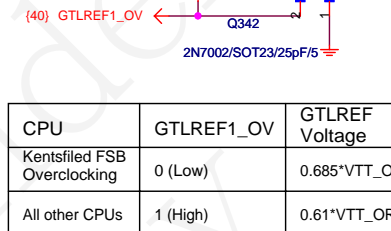
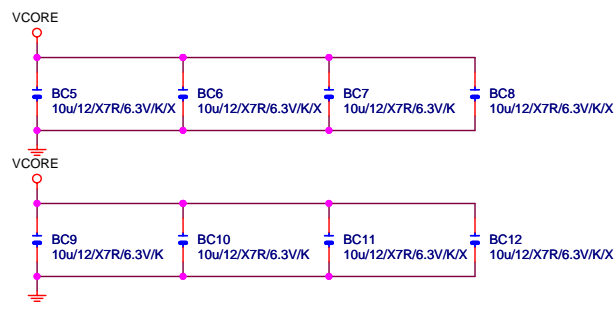
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Circuit or PCB layout change for next version

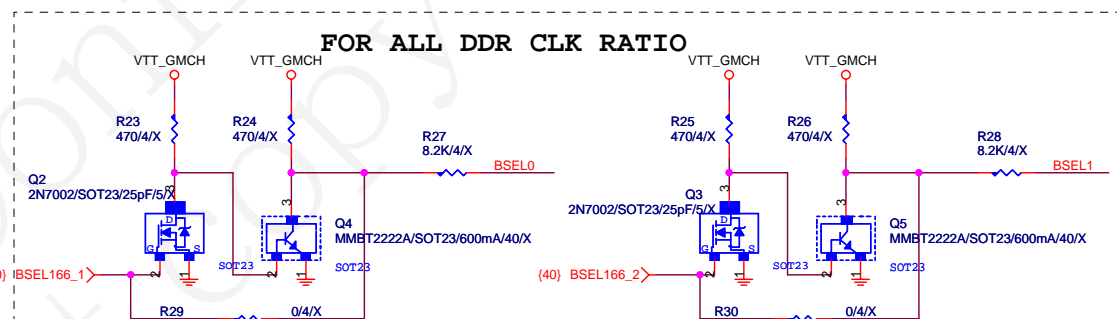
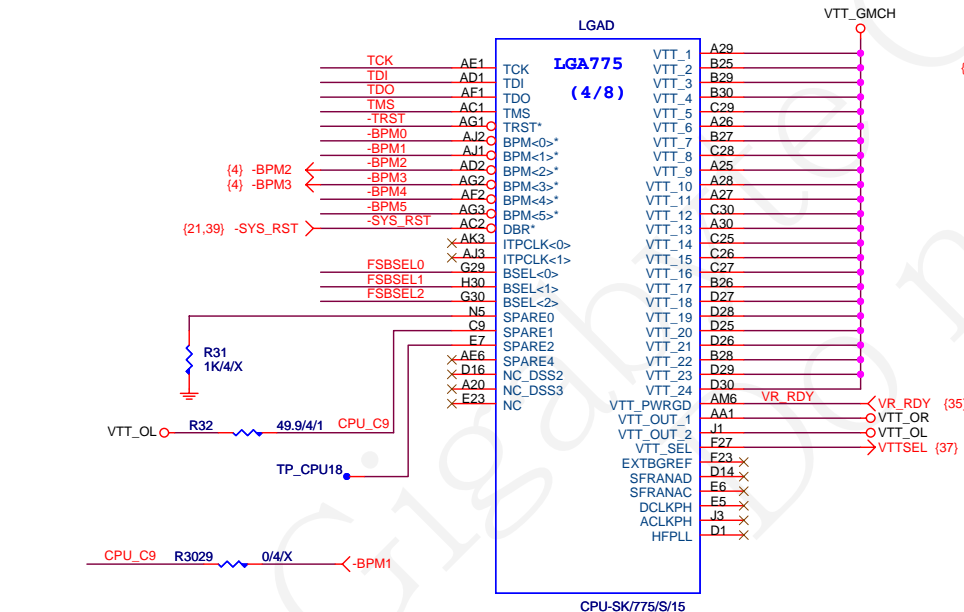
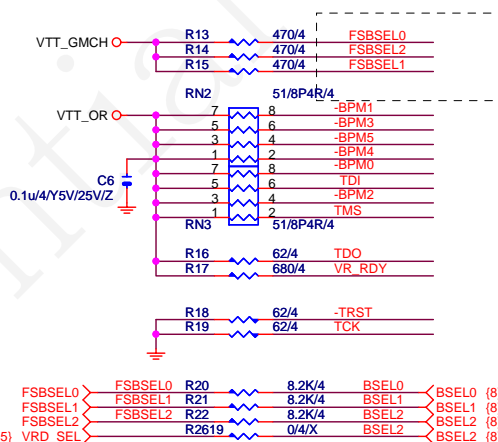
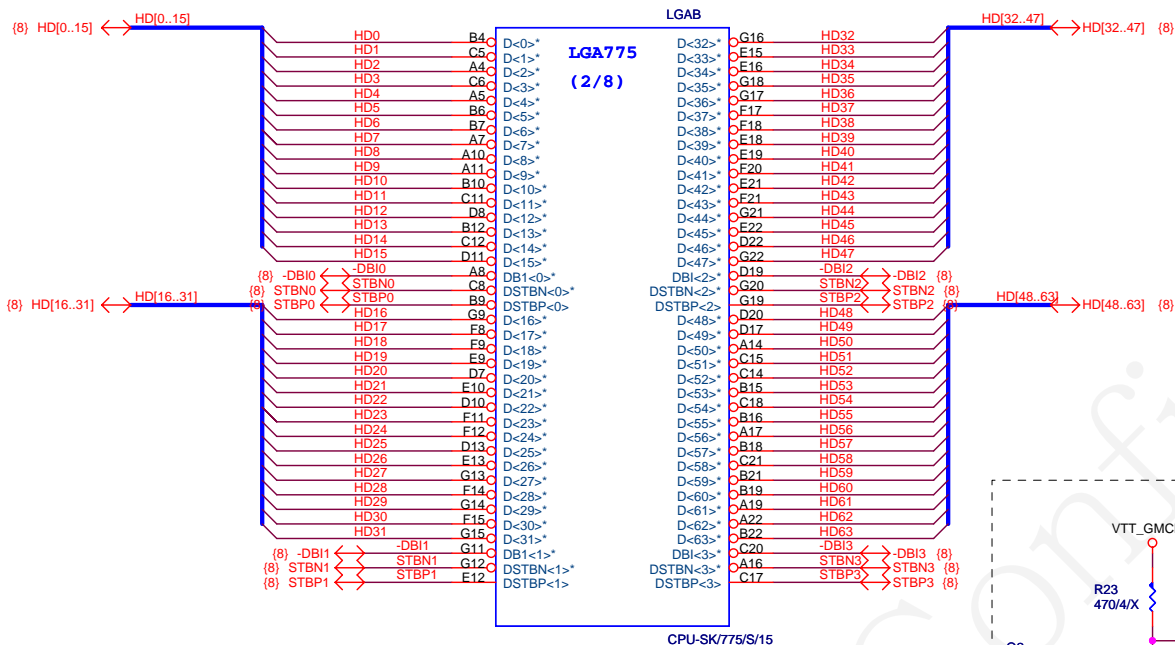
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BLOCK DIAGRAM



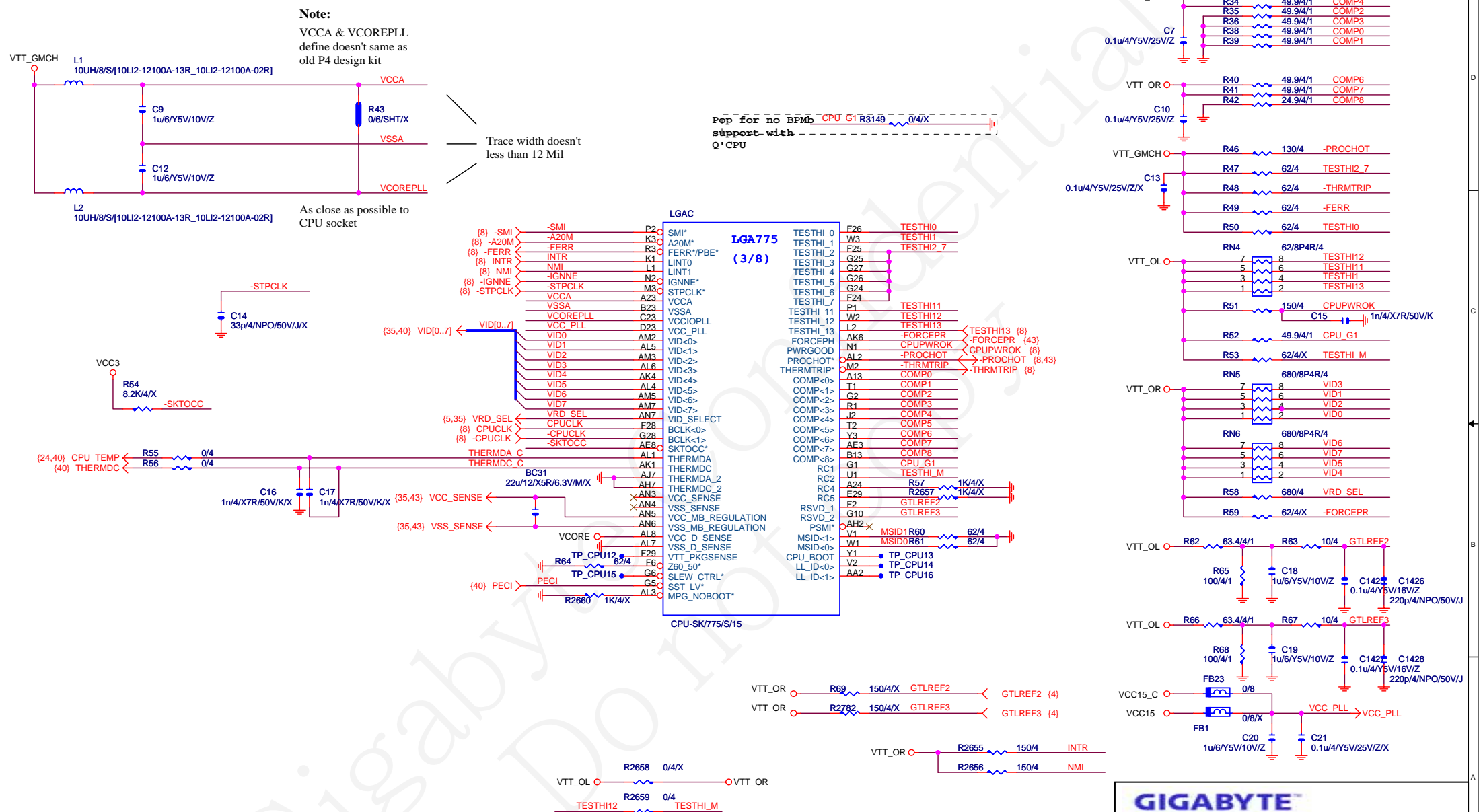


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P4_LGA775-A				
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CHECK BSEL0/1 ITE8712 POWER ON 時電壓是否會高於1.2V
CPU

FSA	FSB	NA	
FSBSEL0	FSBSEL1	FSBSEL2	Clock
1	0	1	100MHz
1	0	0	133MHz
1	1	0	166MHz
0	1	0	200MHz
0	0	0	266MHz

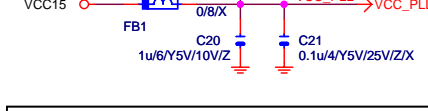
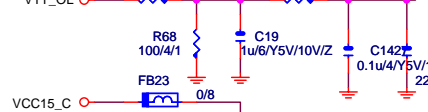
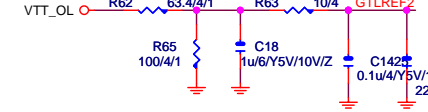
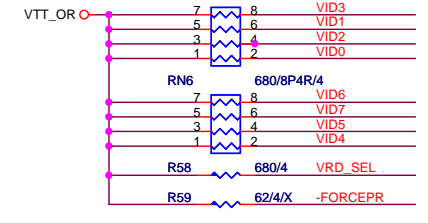
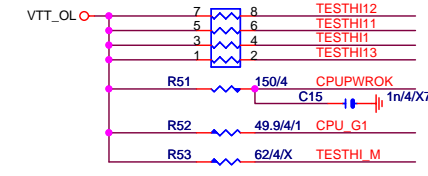
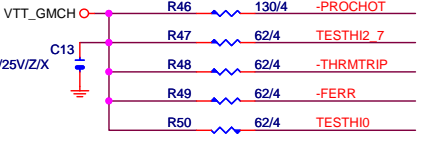
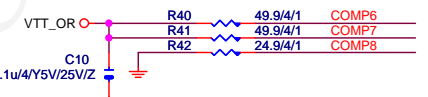
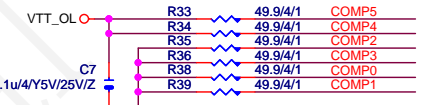


Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit

Trace width doesn't
less than 12 Mil

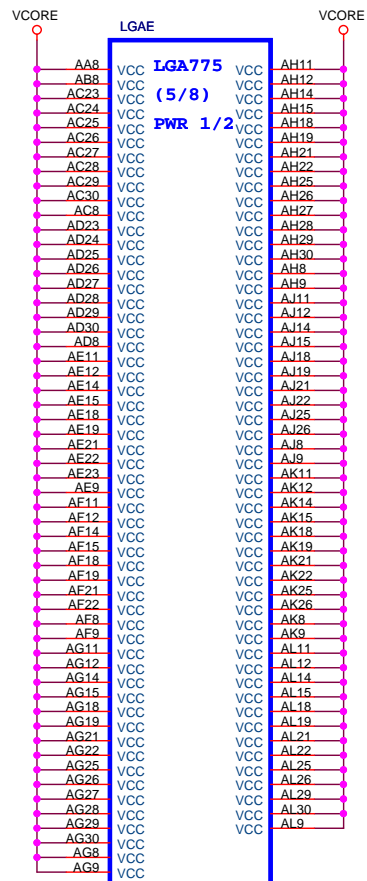
Pop for no BPMB CPU G1 R3149
support with Q' CPU

Place outside of CPU socket

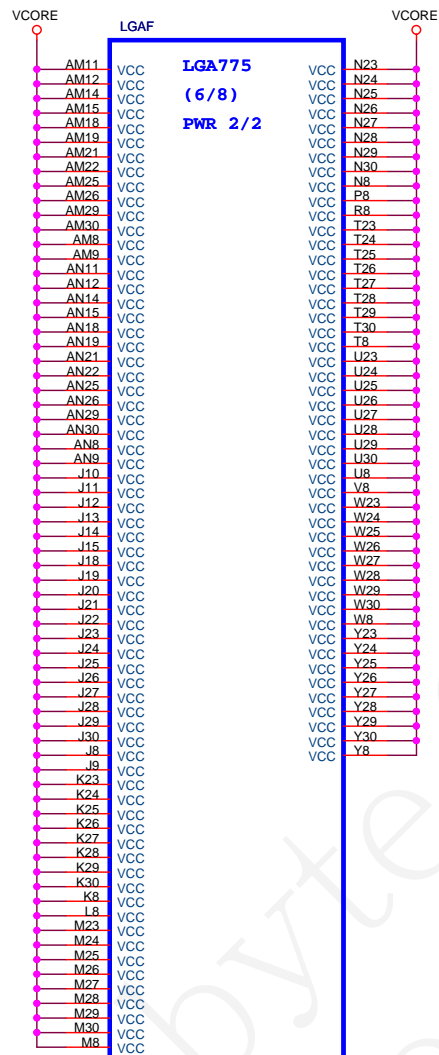


GIGABYTE			
Title			
P4 LGA775-C			
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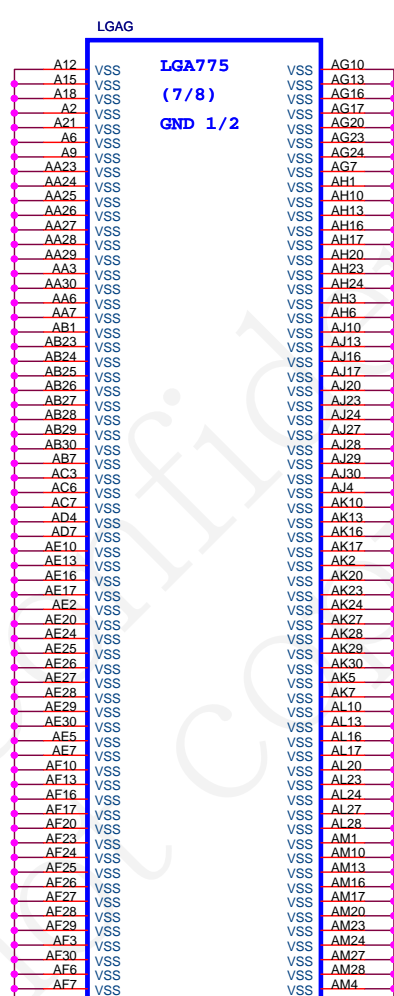
PECI:Platform Environment Control Interface



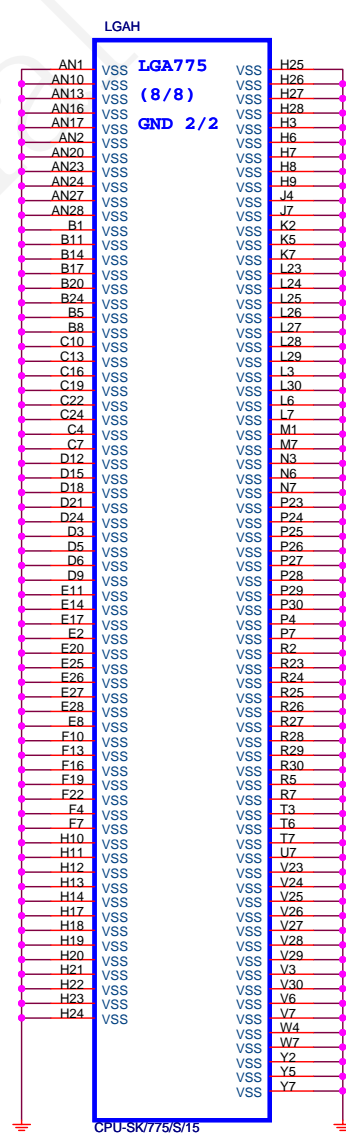
CPU-SK/775/S/15



CPU-SK/775/S/15



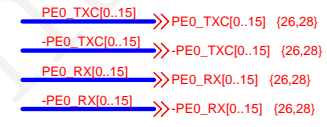
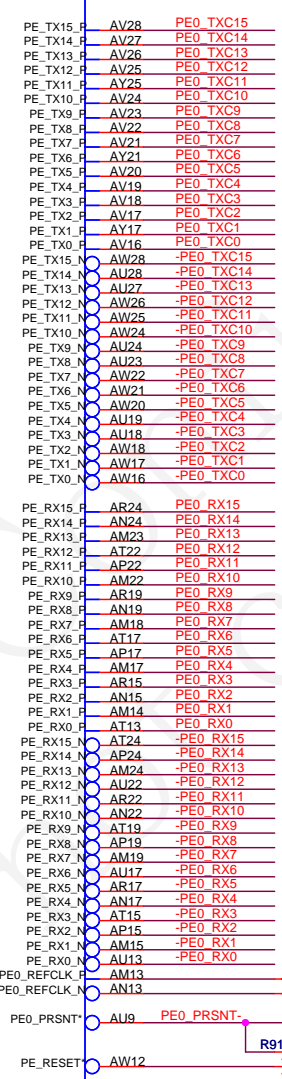
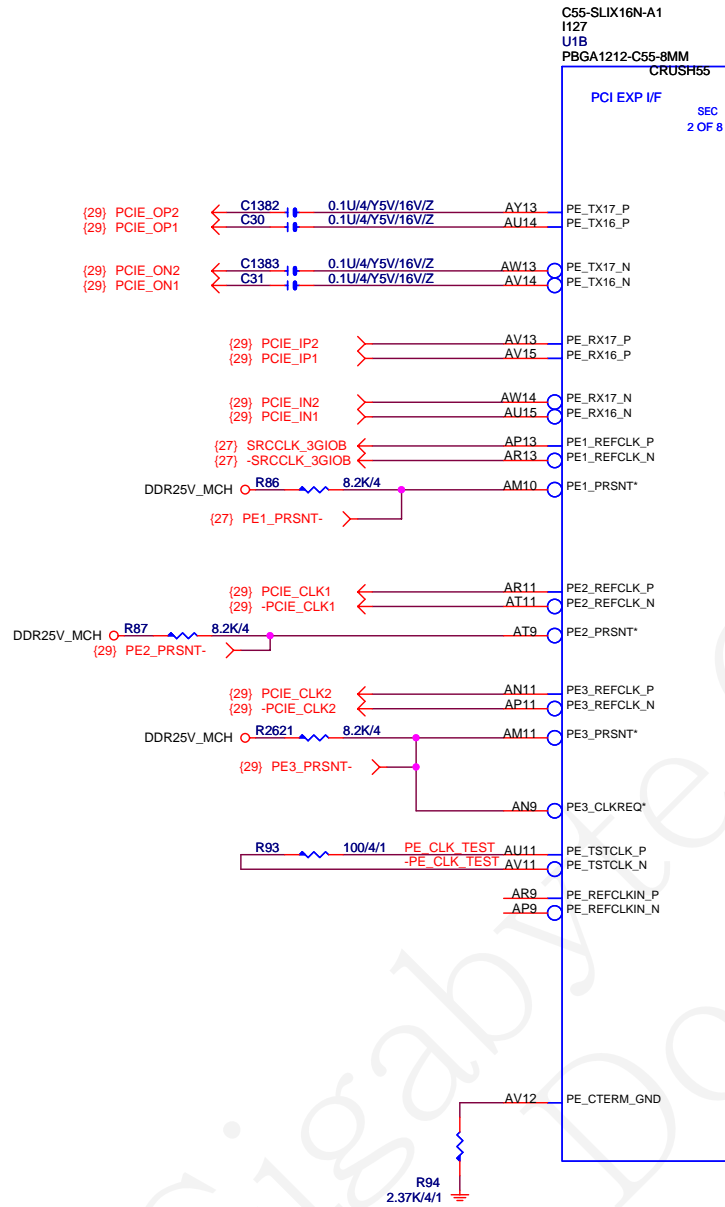
CPU-SK/775/S/15



CPU-SK/775/S/15

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Title		
P4_LGA775-E,F,G,H		
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B	N650SLI-DS4L	1.0
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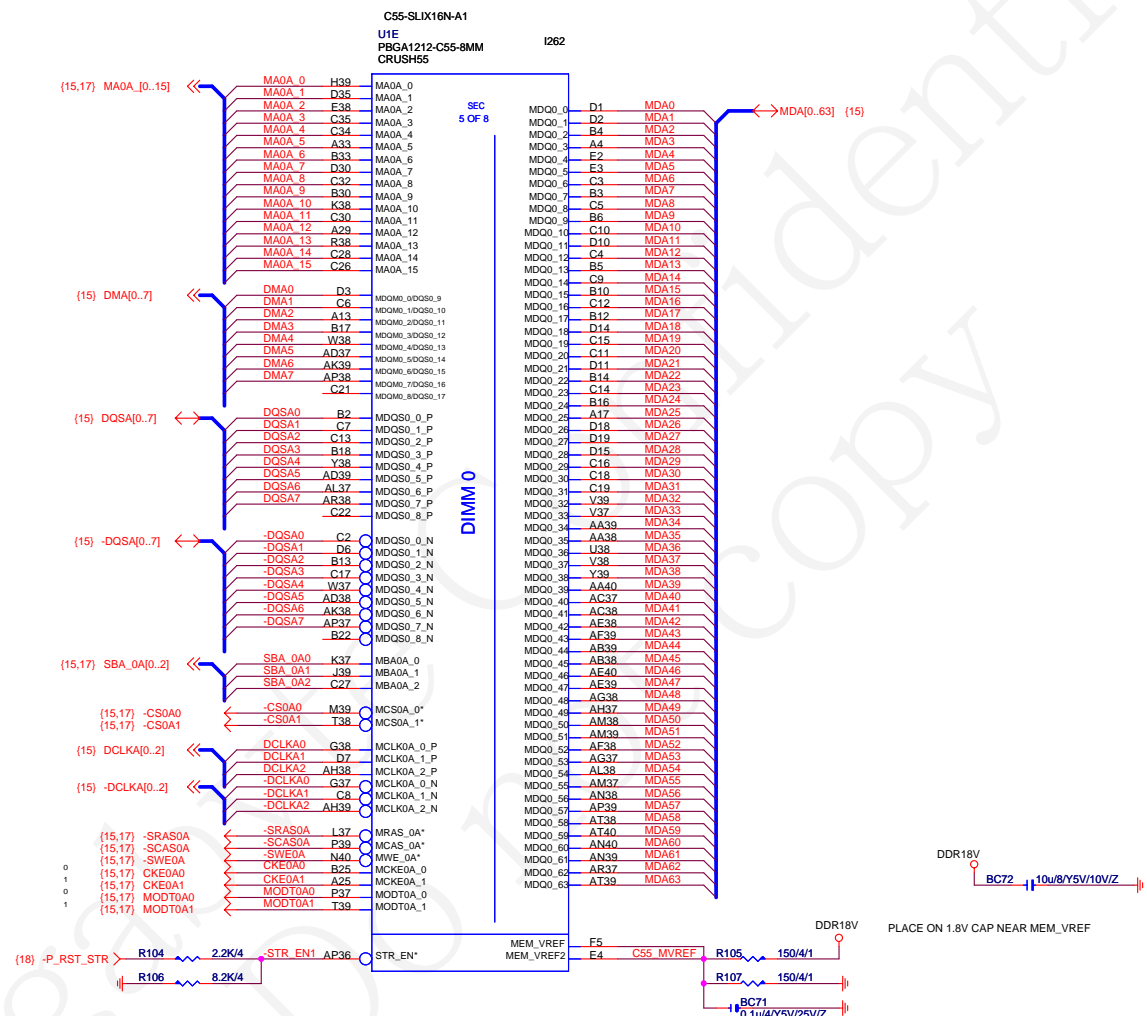


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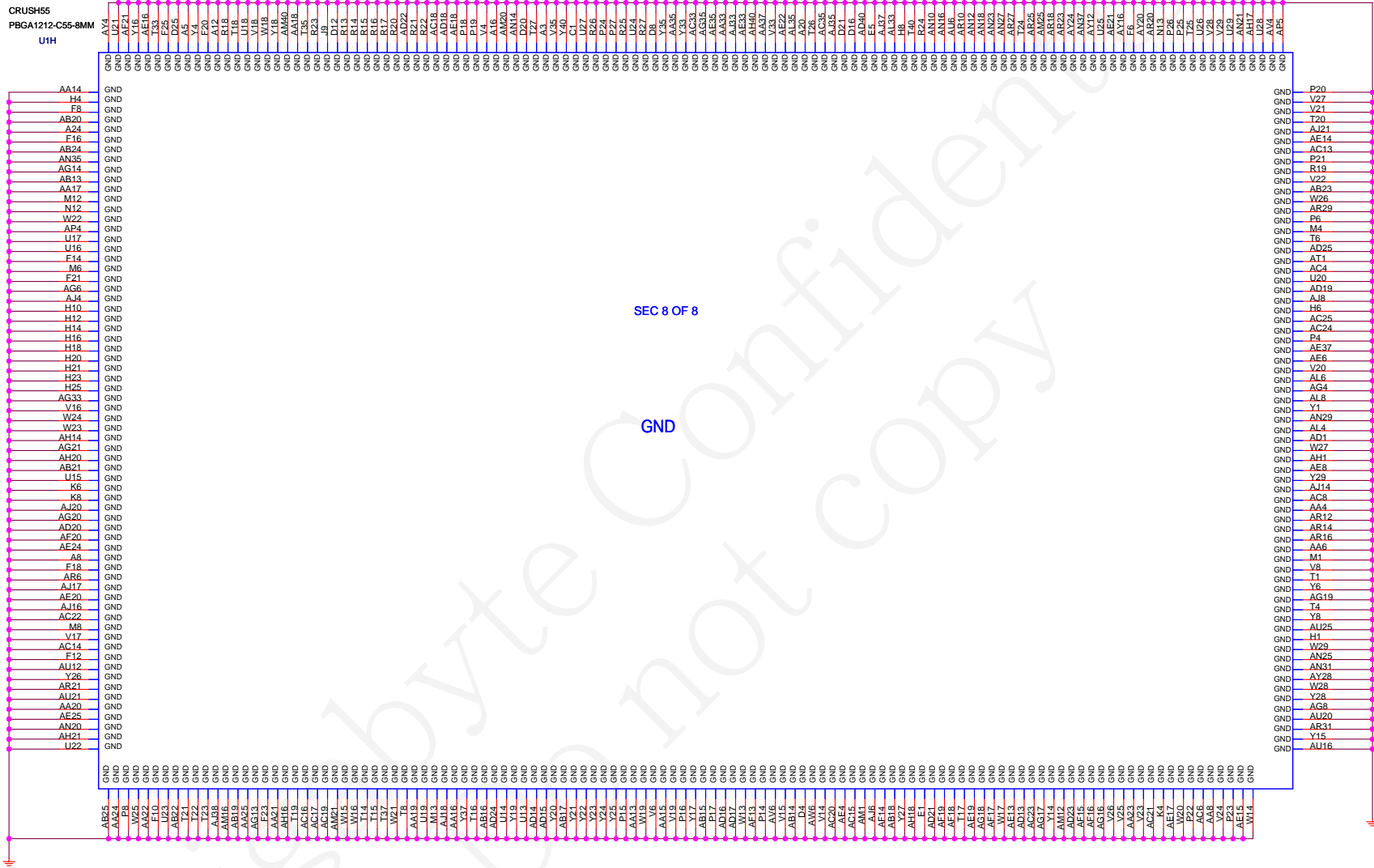
Title
C55_PCIE

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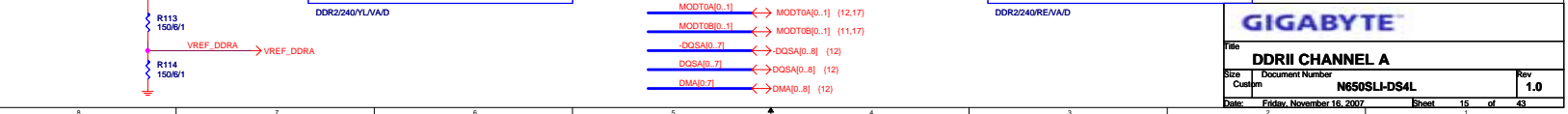
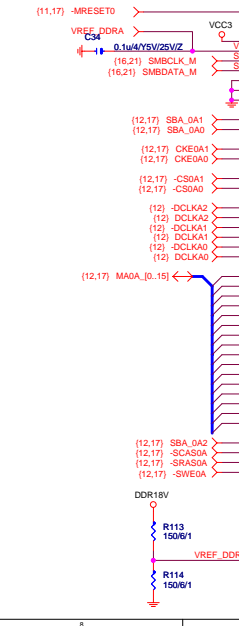
C55-SLIX16N-A1
I231
CRUSH55
PGA1212-C55-8MM
U1H

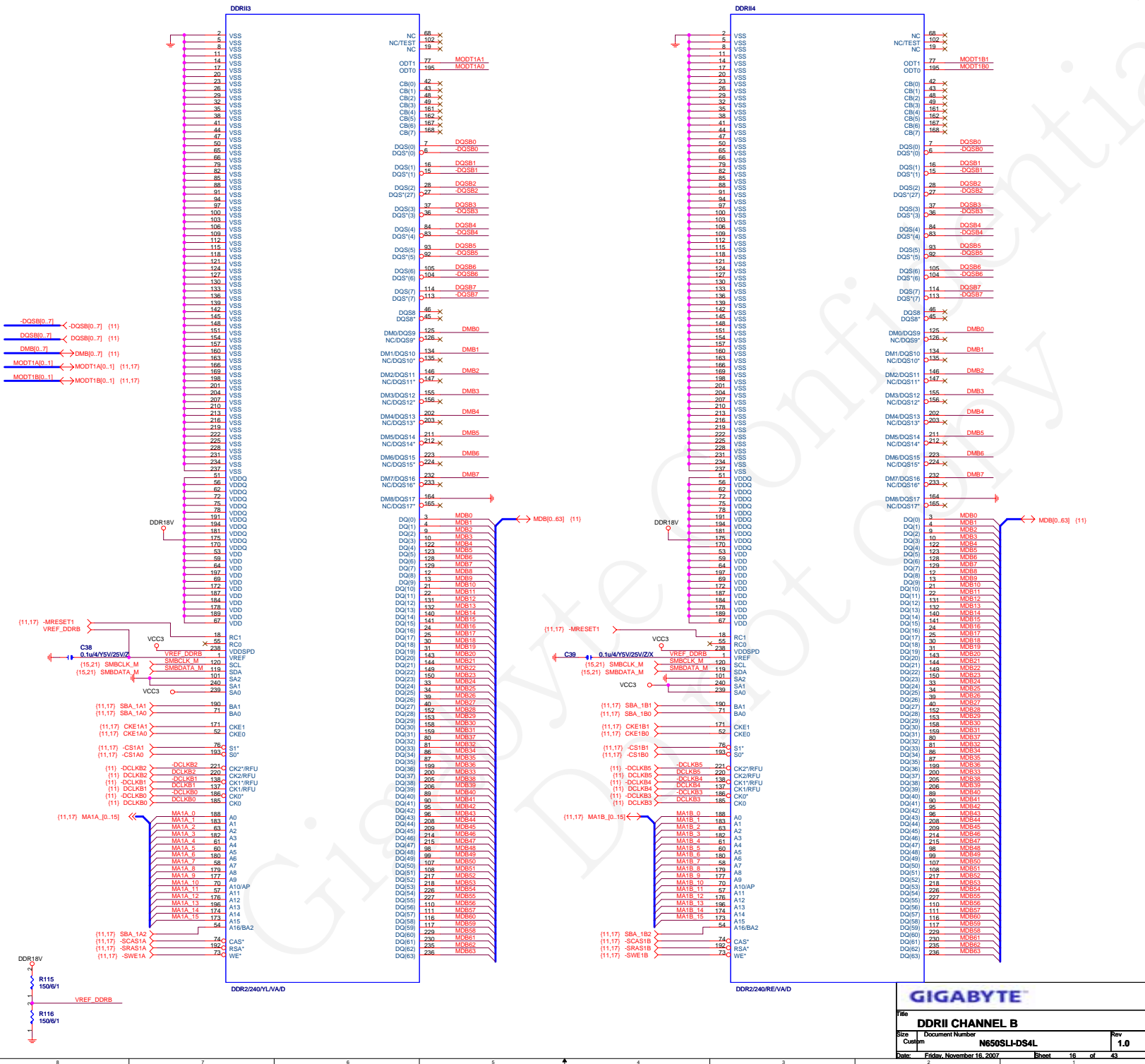


SEC 8 OF 8

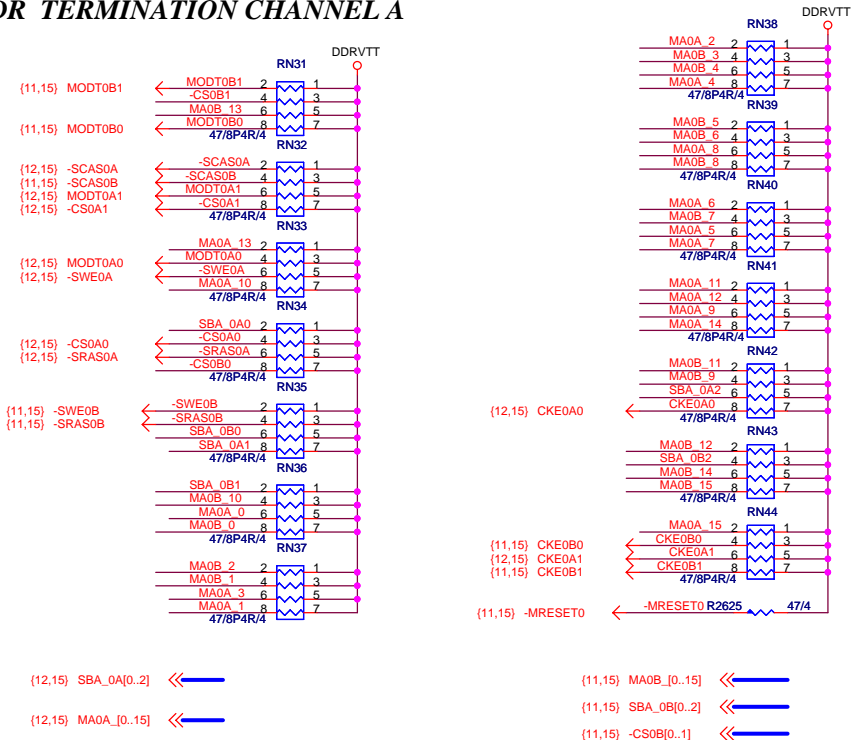
GND

Solder Side Cap

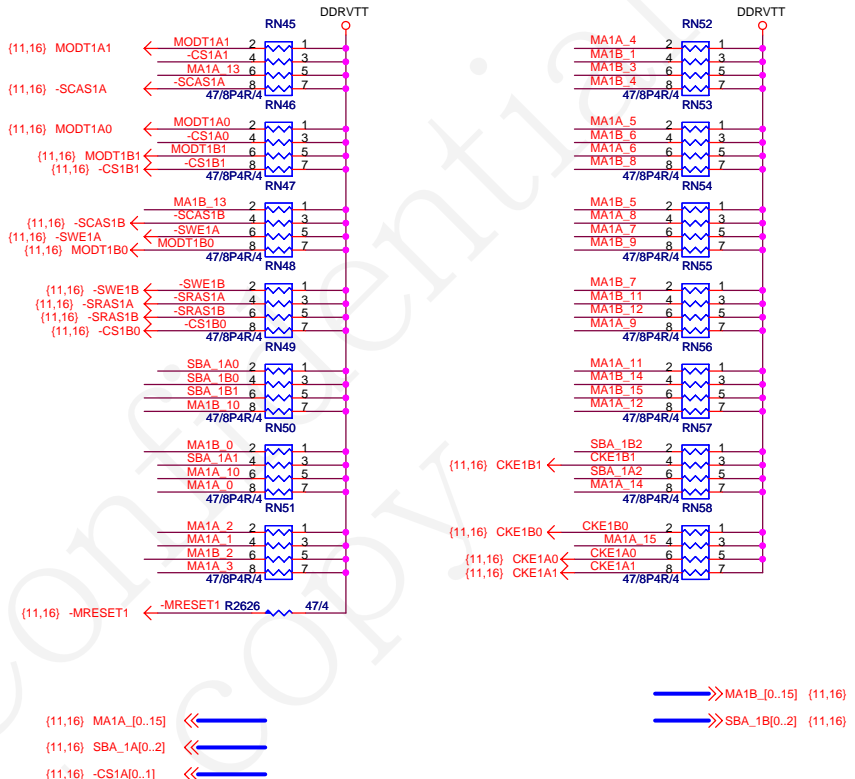




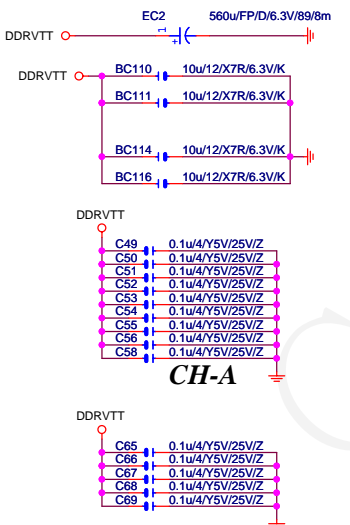
DDR TERMINATION CHANNEL A



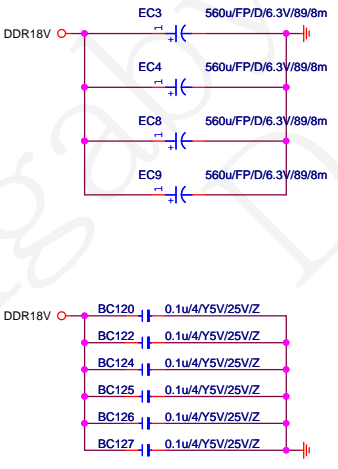
DDRVTT Decouple CHANNEL B



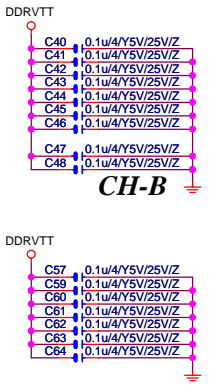
DDRVTT Decouple



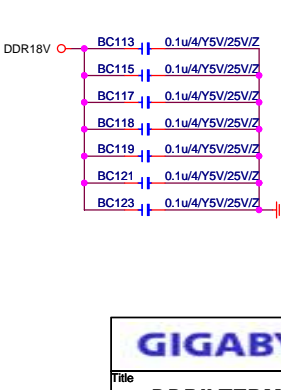
DDR18V Decouple



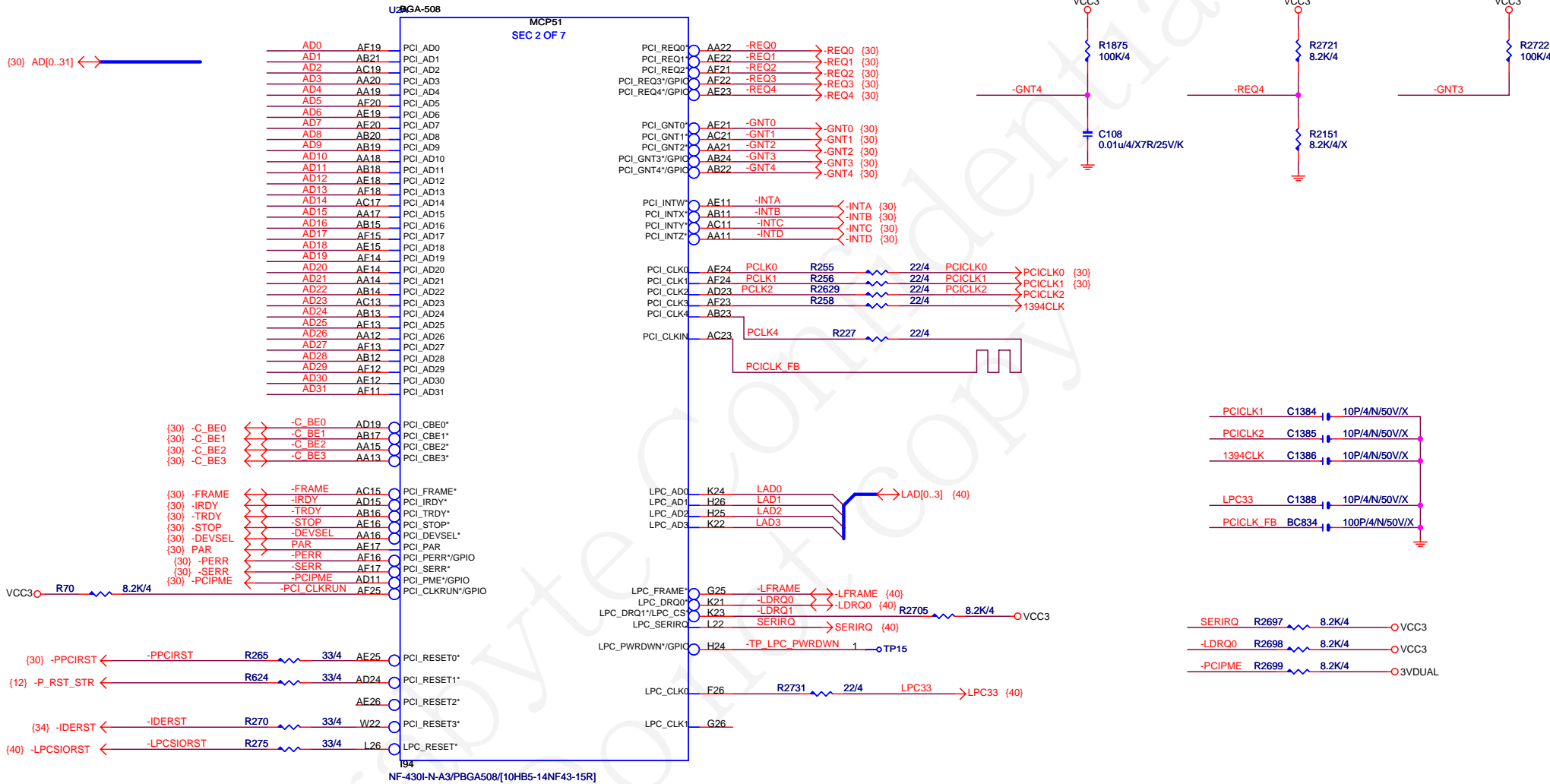
DDRVTT Decouple



DDR18V Decouple



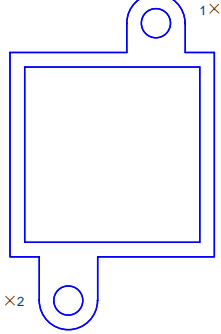
GIGABYTE



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MCP51 PCI BUS			
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S.B FANSINK

SB_HEATSIN



SB_HEATSIN[12SP2-030030-11R_12SP2-030030-12R_12SP2-030030-13R_12SP2-030030-14R]

HT_DWN[0..7] → HT_DWN[0..7] {10}
-HT_DWN[0..7] → -HT_DWN[0..7] {10}

HT_DWN0 K1 HT_MCP_RXD0_P
HT_DWN1 L1 HT_MCP_RXD1_P
HT_DWN2 M1 HT_MCP_RXD2_P
HT_DWN3 N1 HT_MCP_RXD3_P
HT_DWN4 R1 HT_MCP_RXD4_P
HT_DWN5 T1 HT_MCP_RXD5_P
HT_DWN6 U1 HT_MCP_RXD6_P
HT_DWN7 V1 HT_MCP_RXD7_P

-HT_DWN0 K2 HT_MCP_RXD0_N
-HT_DWN1 L2 HT_MCP_RXD1_N
-HT_DWN2 M2 HT_MCP_RXD2_N
-HT_DWN3 N2 HT_MCP_RXD3_N
-HT_DWN4 R2 HT_MCP_RXD4_N
-HT_DWN5 T2 HT_MCP_RXD5_N
-HT_DWN6 U2 HT_MCP_RXD6_N
-HT_DWN7 V2 HT_MCP_RXD7_N

{10} HT_DWN_CLK >> HT_DWN_CLK P1 HT_MCP_RX_CLK_P
{10} -HT_DWN_CLK >> -HT_DWN_CLK P2 HT_MCP_RX_CLK_N

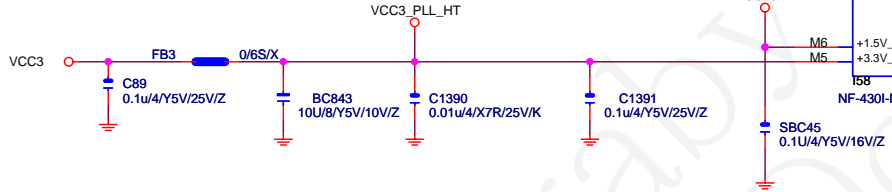
{10} HT_DWN_CTRL >> HT_DWN_CTRL W1 HT_MCP_RXCTL_P
{10} -HT_DWN_CTRL >> -HT_DWN_CTRL W2 HT_MCP_RXCTL_N

{10} -HT_REQ << -HT_REQ AD1 HT_MCP_REQ*
{10} -HT_STOP << -HT_STOP AA5 HT_MCP_STOP*

R2671 150/4 HTMCP_COMP_GND1 AB1 HT_MCP_COMP_GND1
R2672 49.9/4/1 HTMCP_COMP_GND2 AB2 HT_MCP_COMP_GND2

HT1_VLD R302 0/4 HT1VDD_EN

{37} HT1_VLD >> HT1_VLD F22 HT_VLD
{35} VRM_PWRGD >> VRM_PWRGD N26 CPU_VLD
{21,37} -SLP_SS >> MEM_VLD N24 MEM_VLD
{37} HT1VDD_EN >> HT1VDD_EN F23 HTVDD_EN
{37} CPUVDD_EN >> CPUVDD_EN N25 CPUVDD_EN



U2G BGA-508
MCP51
SEC 1 OF 7

HT_MCP_TXD0_P AA1 HT_UP0
HT_MCP_TXD1_P Y1 HT_UP1
HT_MCP_TXD2_P AA3 HT_UP2
HT_MCP_TXD3_P W5 HT_UP3
HT_MCP_TXD4_P U5 HT_UP4
HT_MCP_TXD5_P T5 HT_UP5
HT_MCP_TXD6_P R5 HT_UP6
HT_MCP_TXD7_P P5 HT_UP7

HT_MCP_TXD0_N AA2 -HT_UP0
HT_MCP_TXD1_N Y2 -HT_UP1
HT_MCP_TXD2_N AA4 -HT_UP2
HT_MCP_TXD3_N W6 -HT_UP3
HT_MCP_TXD4_N U6 -HT_UP4
HT_MCP_TXD5_N T6 -HT_UP5
HT_MCP_TXD6_N R6 -HT_UP6
HT_MCP_TXD7_N P6 -HT_UP7

HT_MCP_TX_CLK_P V5 HT_UP_CLK >> HT_UP_CLK {10}
HT_MCP_TX_CLK_N V6 -HT_UP_CLK >> -HT_UP_CLK {10}

HT_MCP_TXCTL_P N5 HT_UP_CTRL >> HT_UP_CTRL {10}
HT_MCP_TXCTL_N N6 -HT_UP_CTRL >> -HT_UP_CTRL {10}

CLKOUT_200MHZ_P AC1 << C55_CLK {10}
CLKOUT_200MHZ_N AC2 << -C55_CLK {10}

CLKOUT_25MHZ Y5 << C55_25MHZ_IN {10}
HT_MCP_PWRGD AD2 HT_PWRGD >> HT_PWRGD {10}
HT_MCP_RST* AE1 -HT_RESET1 >> -HT_RESET {10}
THERMTRIP*GPIO J6 << VCC3
CLK200MHZ_TERM_GND K6 << CLK200MHZ_TERM_GND

HT_UP[0..7] → HT_UP[0..7] {10}
-HT_UP[0..7] → -HT_UP[0..7] {10}

-HT_RESET1 R2781 8.2K/4 VCC3

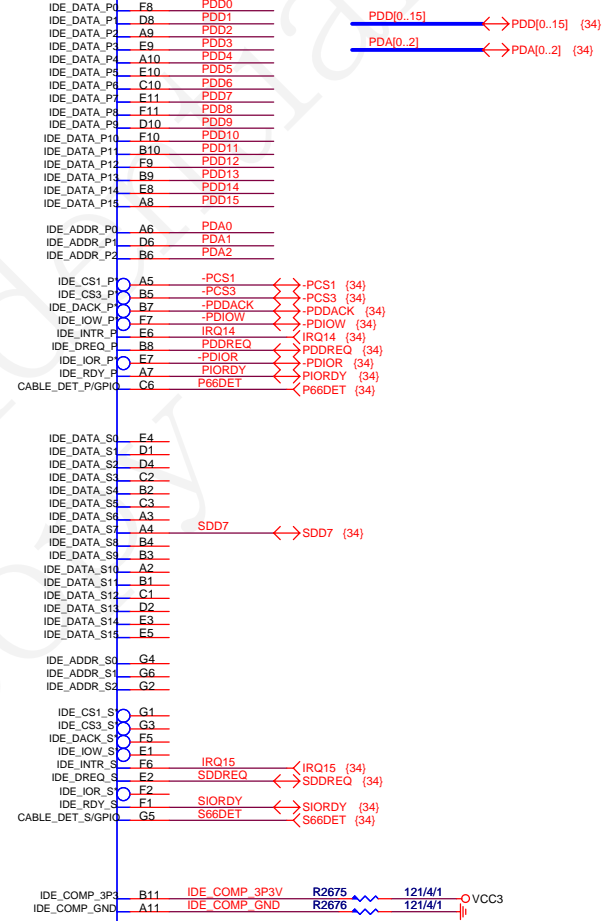
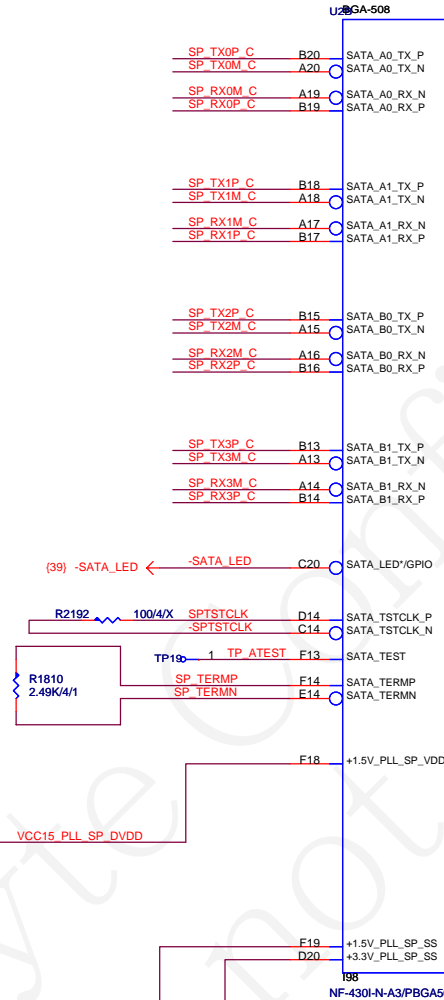
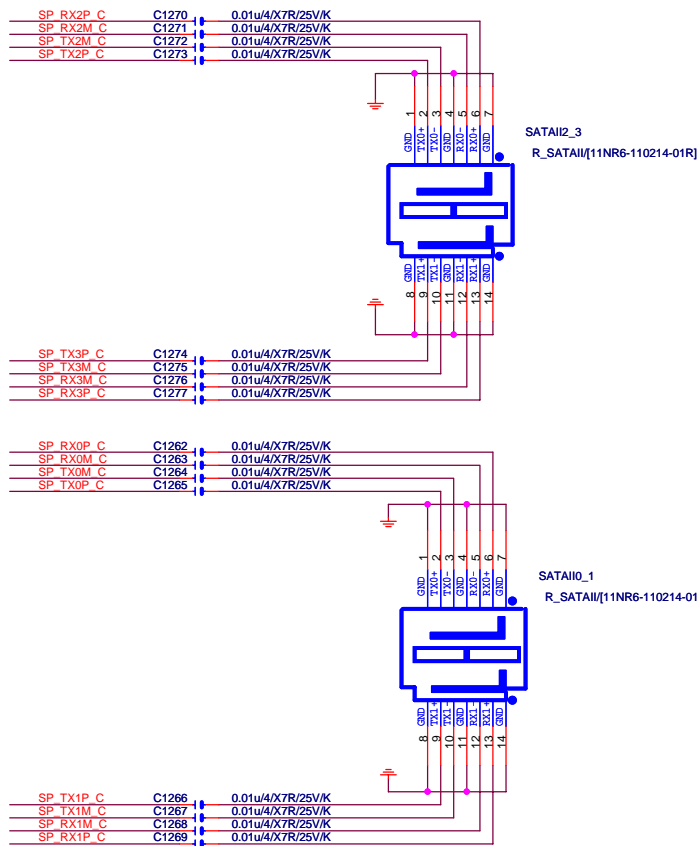
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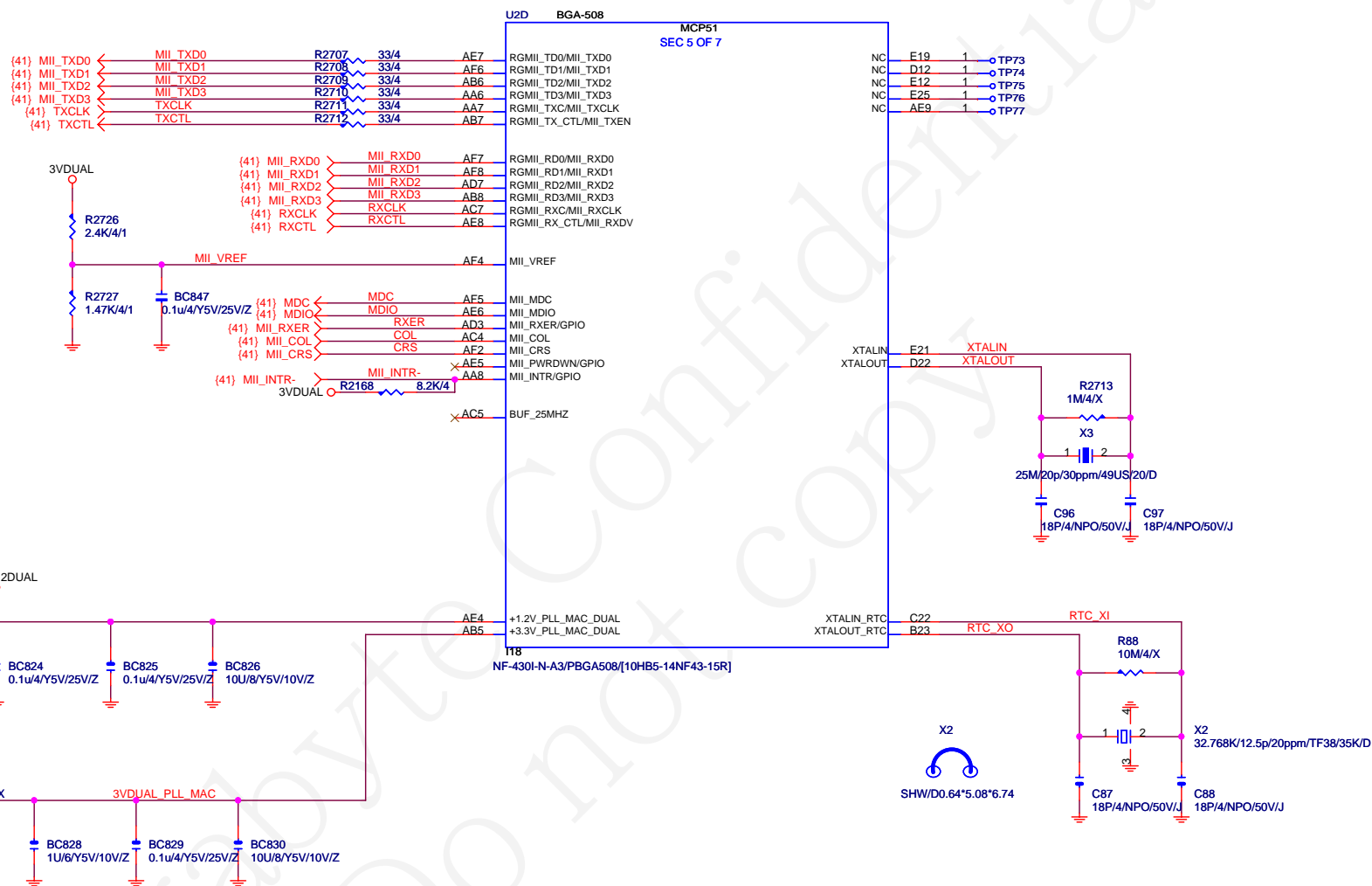
JTAG_TCK H22 MCP51_TCK R2135 8.2K/4
JTAG_TDI H21 MCP51_TDI R2136 8.2K/4
JTAG_TDO H23 TP MCP51_TDO R2137 8.2K/4
JTAG_TMS D26 MCP51_TMS
JTAG_TRST* F25 MCP51_TRST* R2138 8.2K/4

NF-430I-N-A3/PBGA508[10HB5-14NF43-15R]

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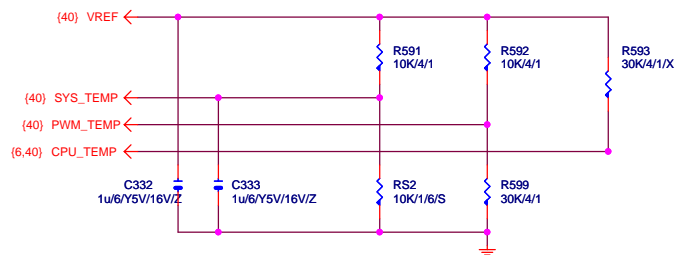
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MCP51 HT		
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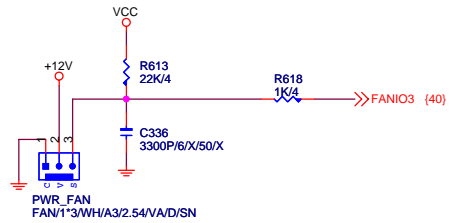
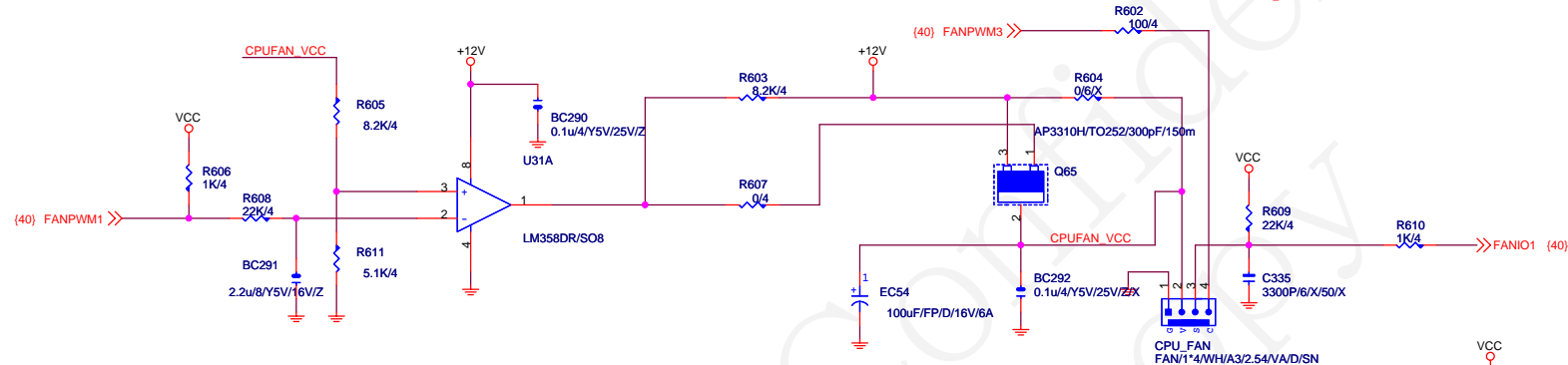
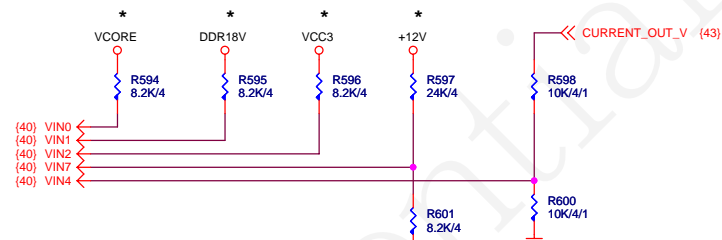


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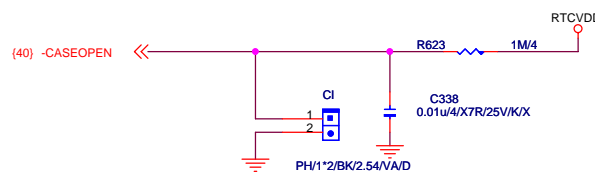
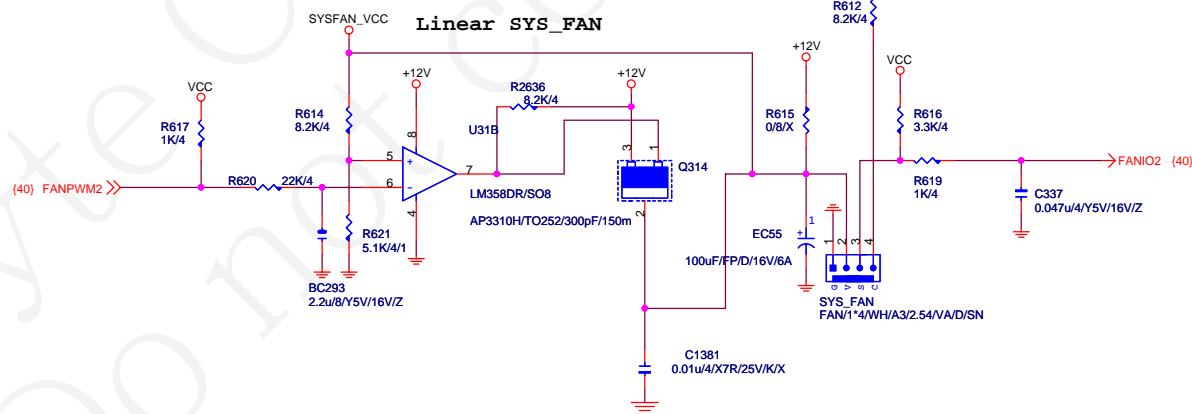
Title		
MCP51 RGMII		
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VOLTAGE-- H/W MONITOR

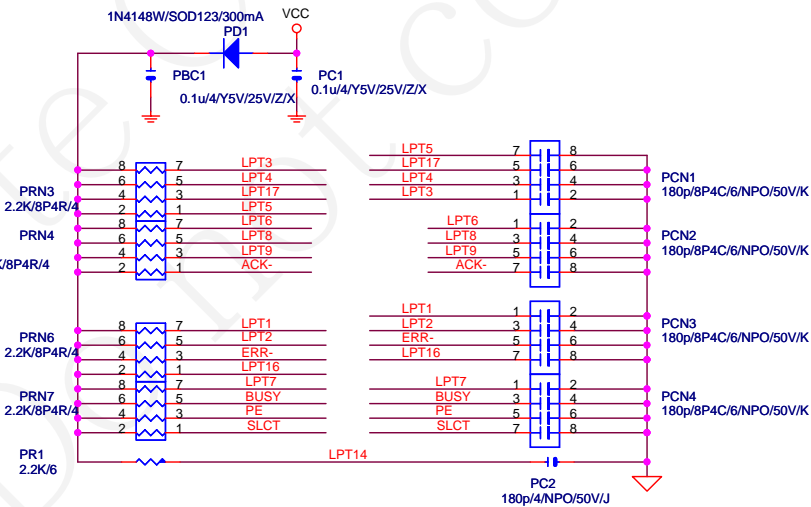
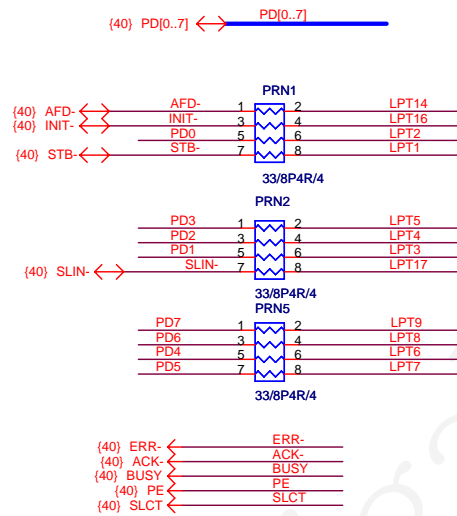
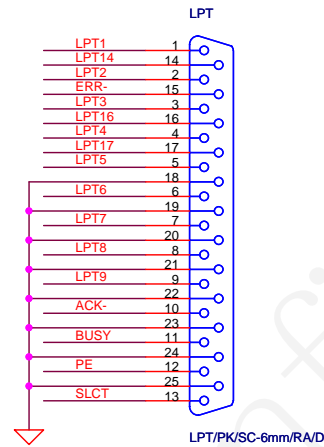


SYS_FAN

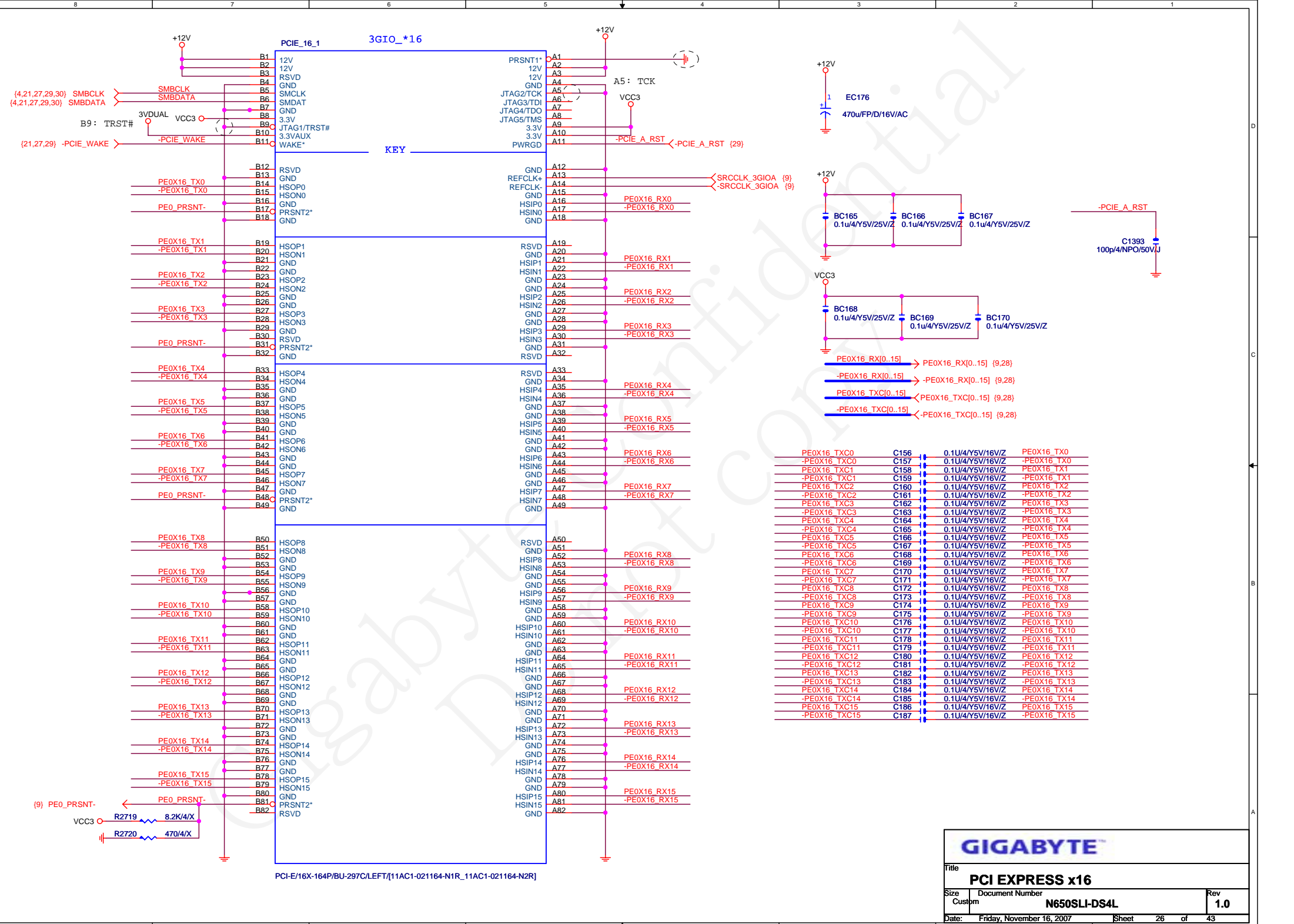


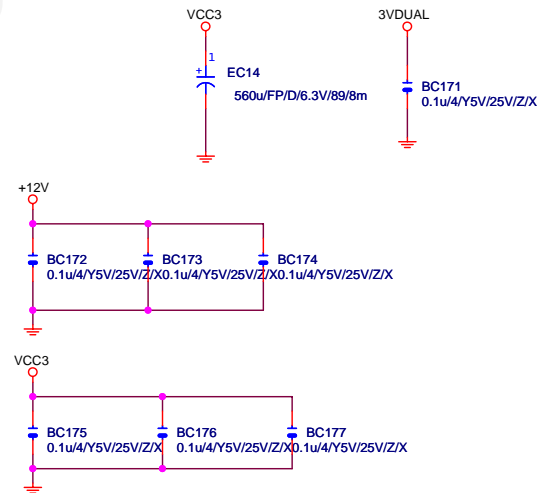
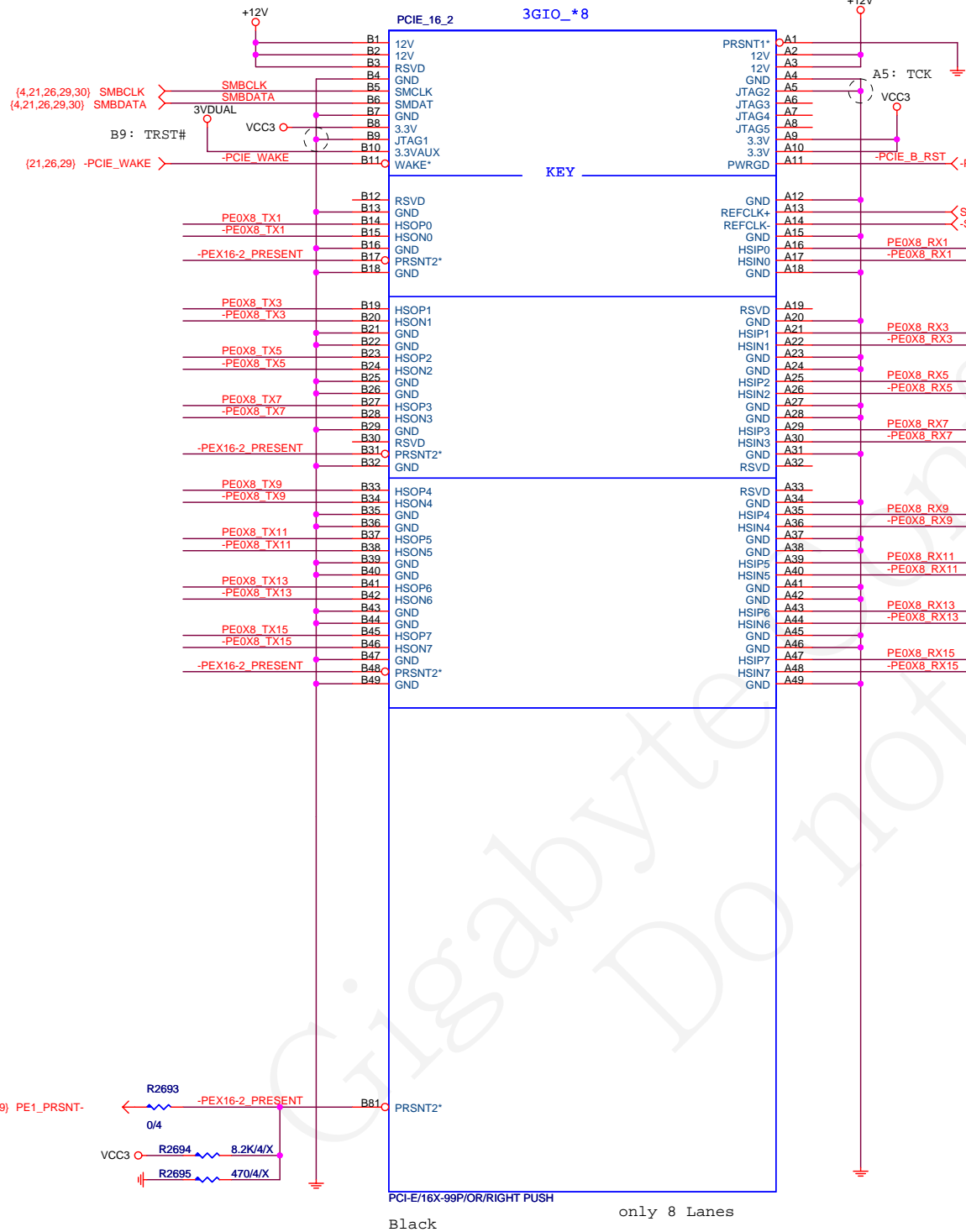
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FAN/HWMO		
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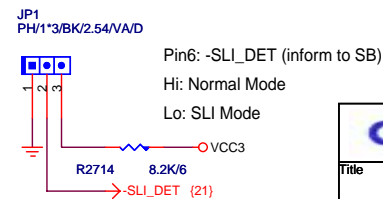
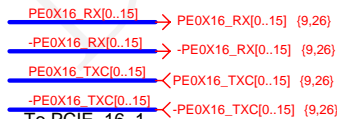
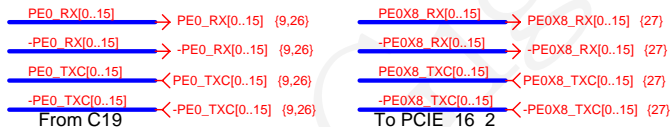
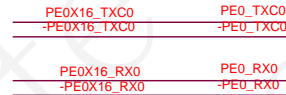
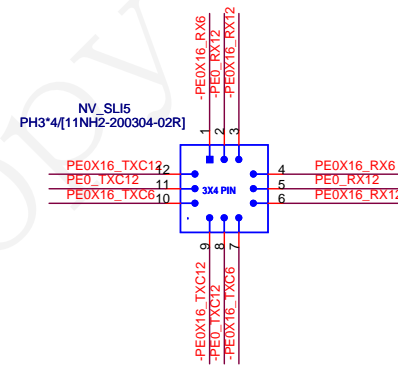
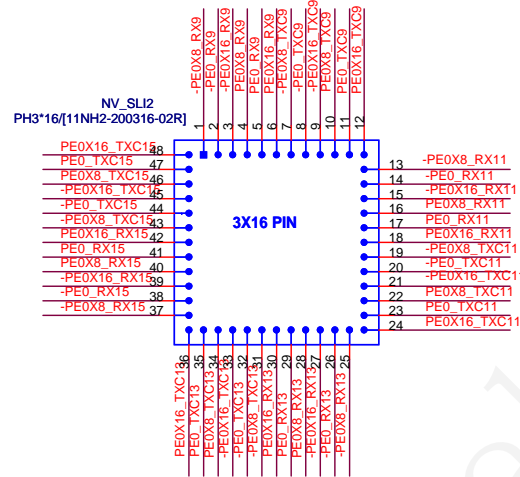
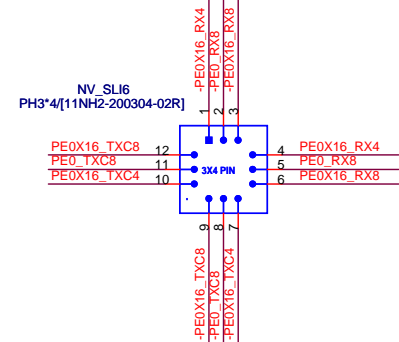
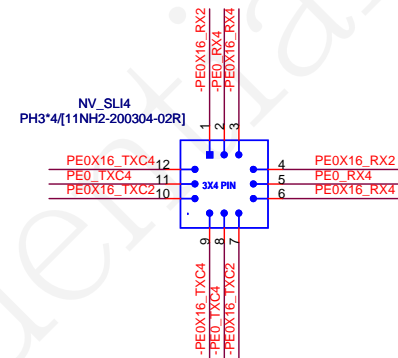
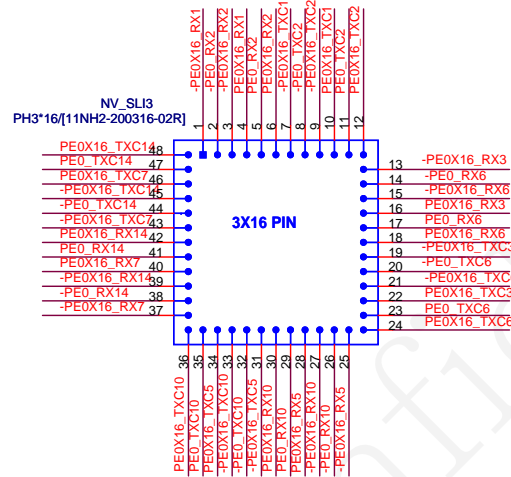
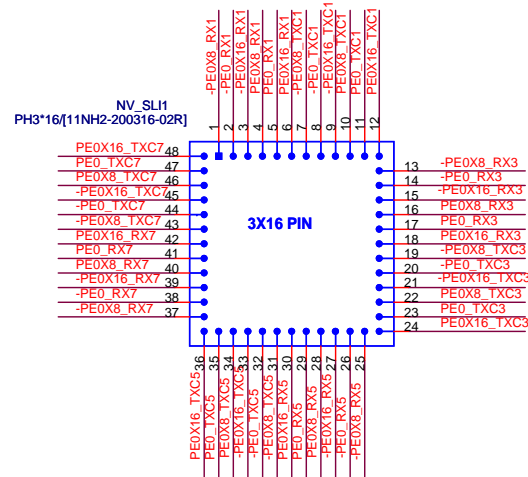


GIGABYTE™			
Title LPT			
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PE0X8_TXC1	C189	0.1U/4/Y5V/16V/Z	PE0X8_TX1
-PE0X8_TXC1	C190	0.1U/4/Y5V/16V/Z	-PE0X8_TX1
PE0X8_TXC3	C191	0.1U/4/Y5V/16V/Z	PE0X8_TX3
-PE0X8_TXC3	C192	0.1U/4/Y5V/16V/Z	-PE0X8_TX3
PE0X8_TXC5	C193	0.1U/4/Y5V/16V/Z	PE0X8_TX5
-PE0X8_TXC5	C194	0.1U/4/Y5V/16V/Z	-PE0X8_TX5
PE0X8_TXC7	C195	0.1U/4/Y5V/16V/Z	PE0X8_TX7
-PE0X8_TXC7	C196	0.1U/4/Y5V/16V/Z	-PE0X8_TX7
PE0X8_TXC9	C197	0.1U/4/Y5V/16V/Z	PE0X8_TX9
-PE0X8_TXC9	C198	0.1U/4/Y5V/16V/Z	-PE0X8_TX9
PE0X8_TXC11	C199	0.1U/4/Y5V/16V/Z	PE0X8_TX11
-PE0X8_TXC11	C200	0.1U/4/Y5V/16V/Z	-PE0X8_TX11
PE0X8_TXC13	C201	0.1U/4/Y5V/16V/Z	PE0X8_TX13
-PE0X8_TXC13	C202	0.1U/4/Y5V/16V/Z	-PE0X8_TX13
PE0X8_TXC15	C203	0.1U/4/Y5V/16V/Z	PE0X8_TX15
-PE0X8_TXC15	C204	0.1U/4/Y5V/16V/Z	-PE0X8_TX15

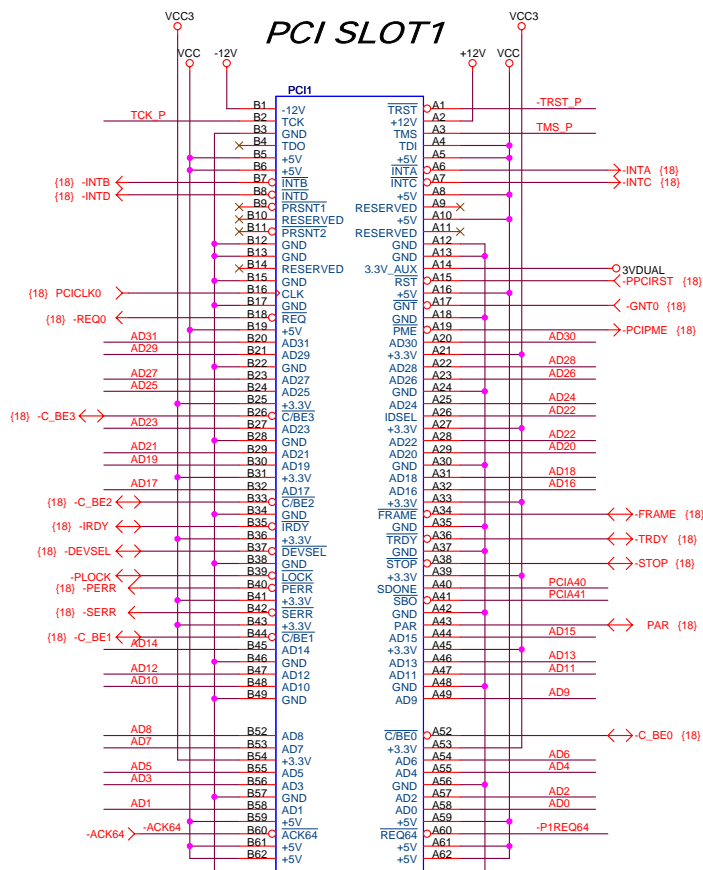


GIGABYTE		
Title NV_SLI CONNECTOR		
Size B	Document Number N650SLI-DS4L	Rev 1.0
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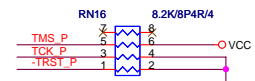
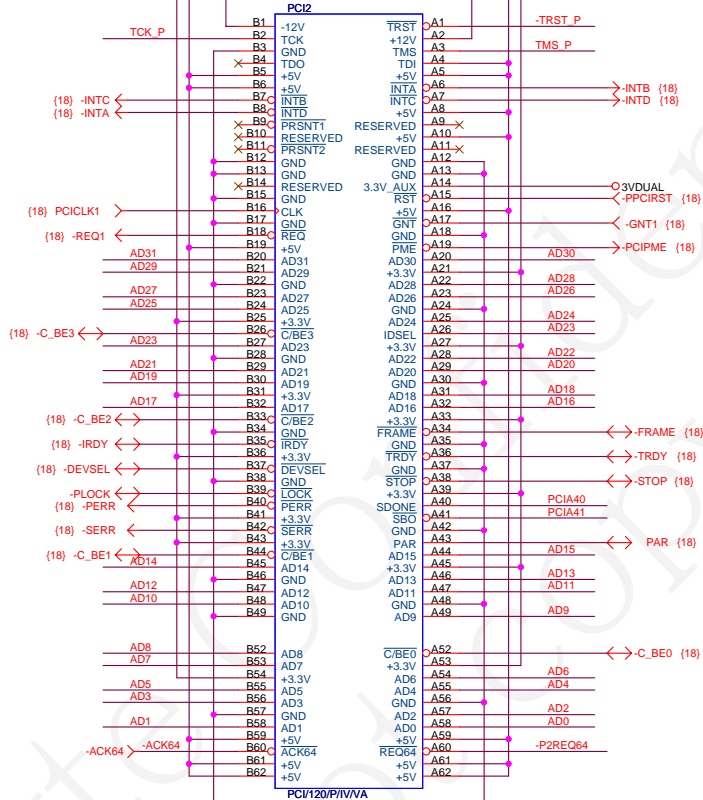
PCI SLOT 1,2

PCI SLOT1

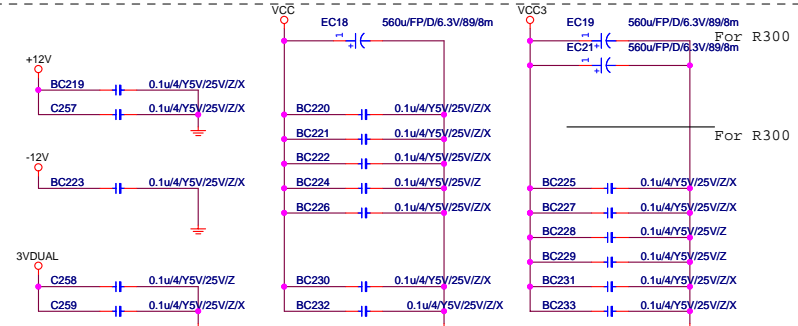
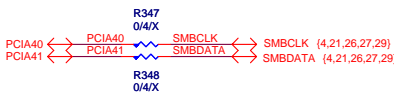
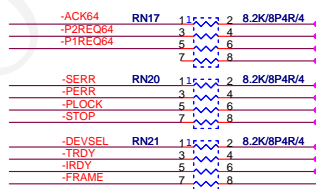
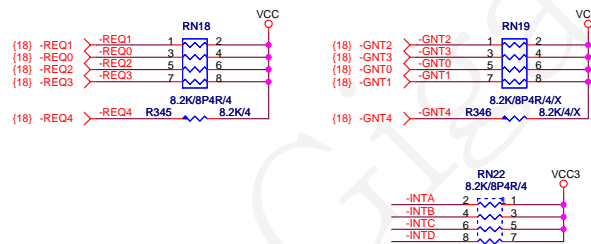
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PCI SLOT2

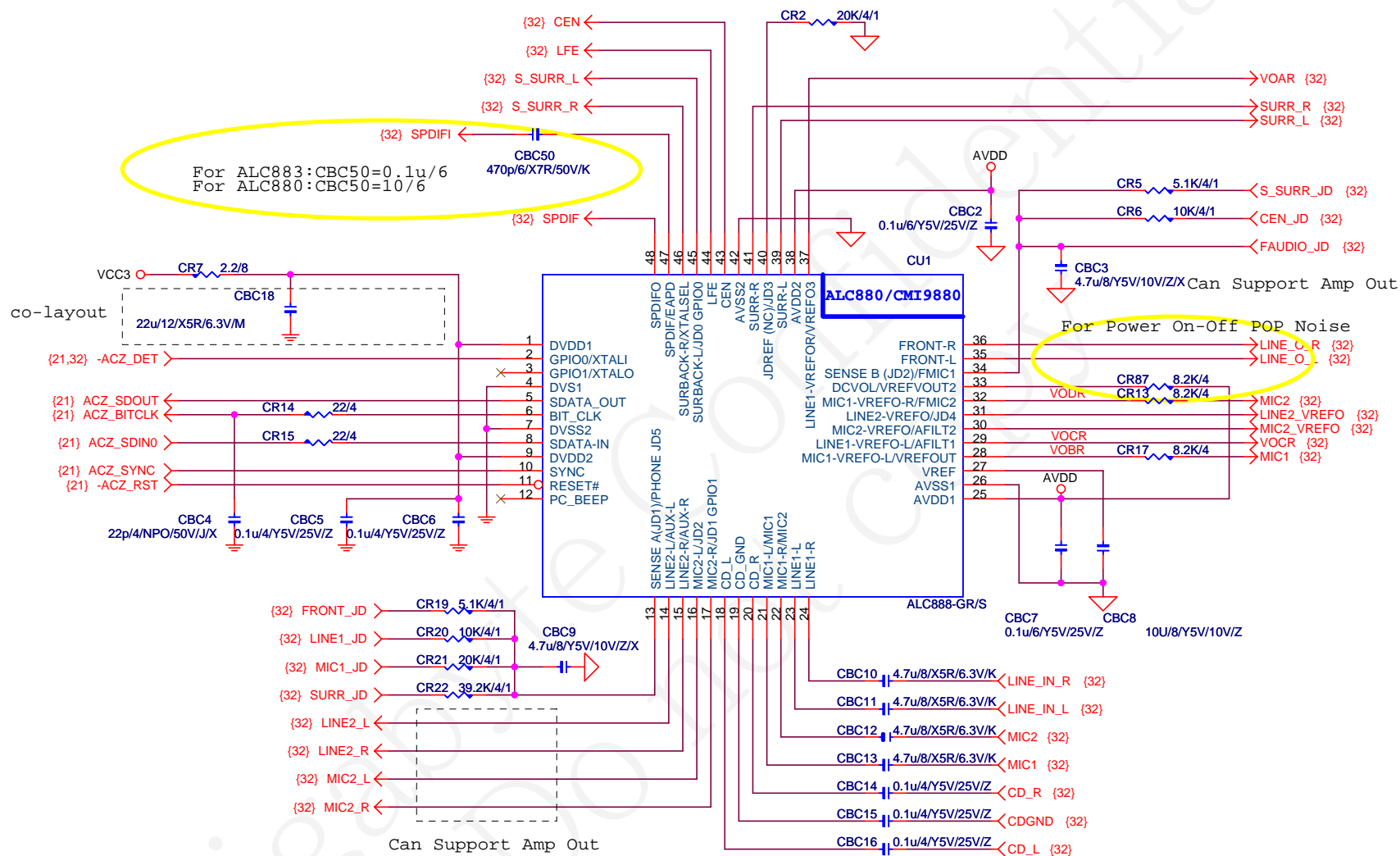


IDSEL(A23)
(D)



GIGABYTE

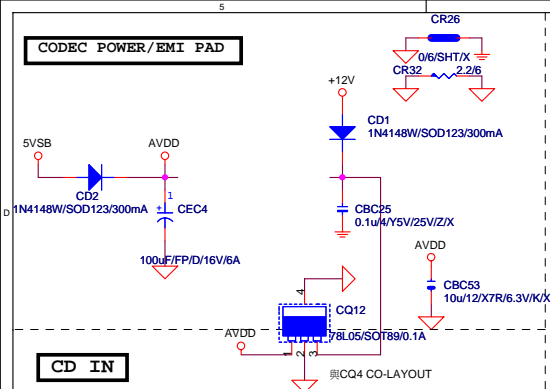
OCI SOT 1, 2, 3		
Size	Document Number	Rev
Custom	N650SLI-DS4L	1.0
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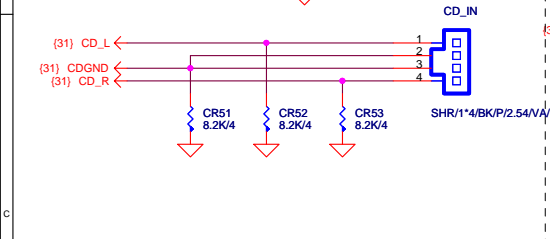
GIGABYTE

Title			
CODEC ALC888			
Size	Document Number	Rev	
Custom	N650SLI-DS4L	1.0	
Date:	Friday, November 16, 2007	Sheet	31 of 43

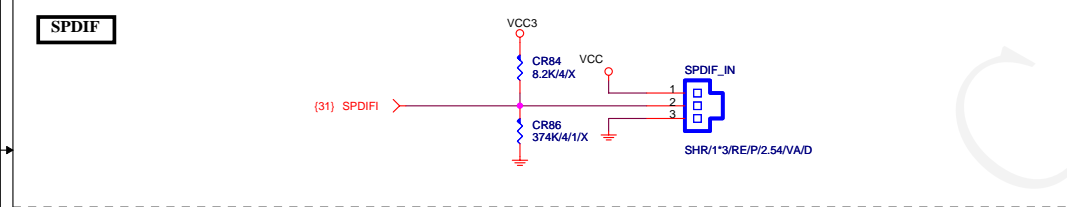
CODEC POWER/EMI PAD



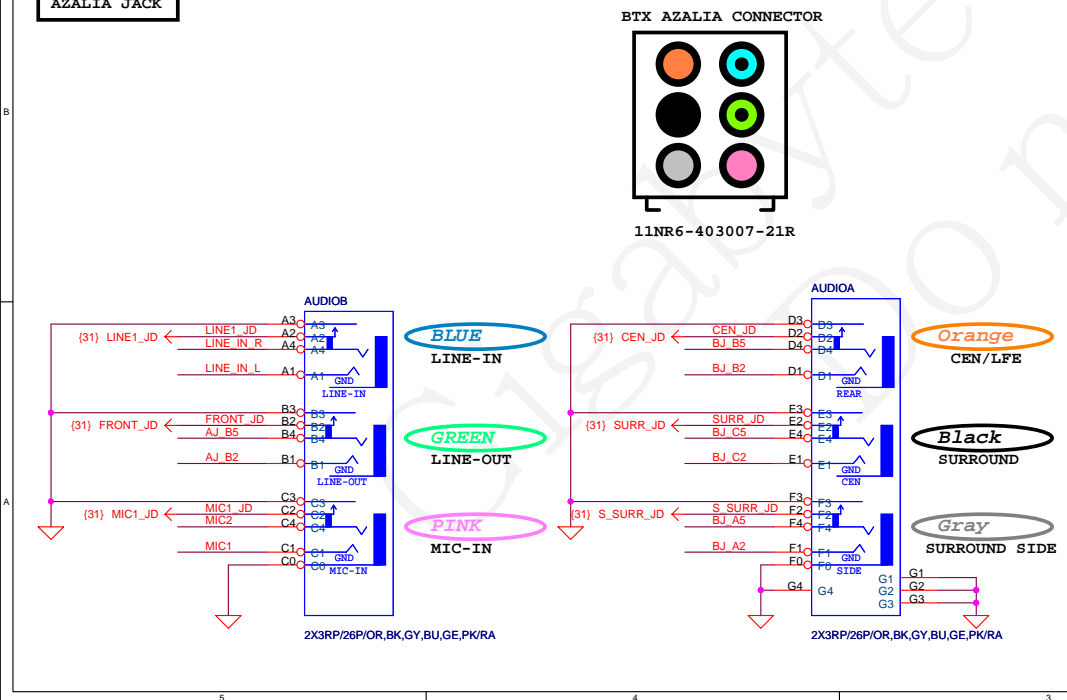
CD IN



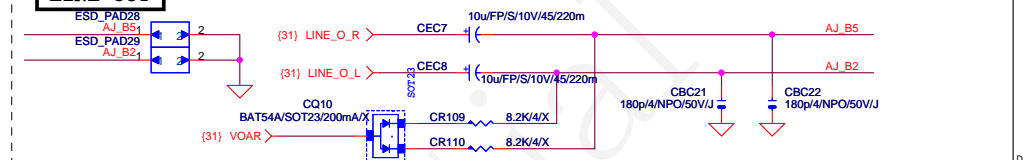
SPDIF



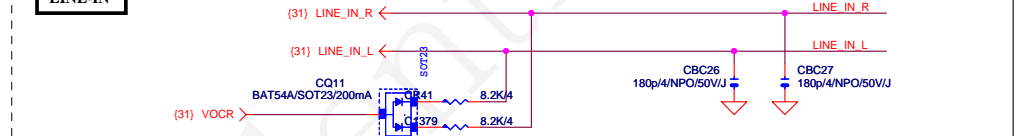
AZALIA JACK



LINE-OUT



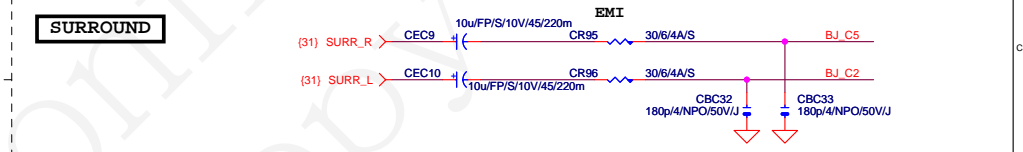
LINE-IN



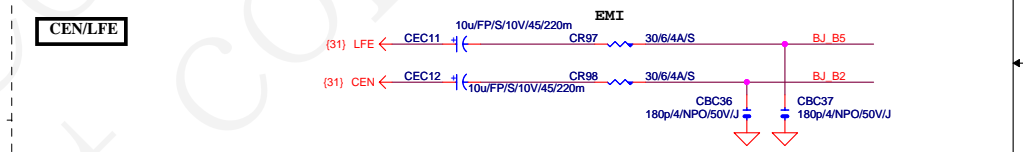
MIC-IN



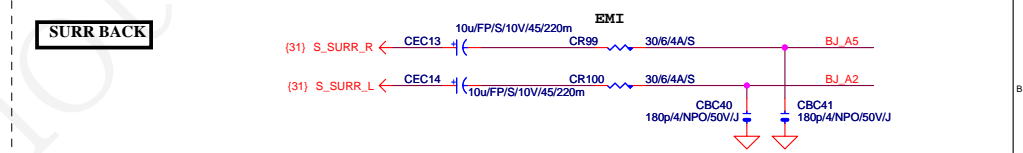
SURROUND



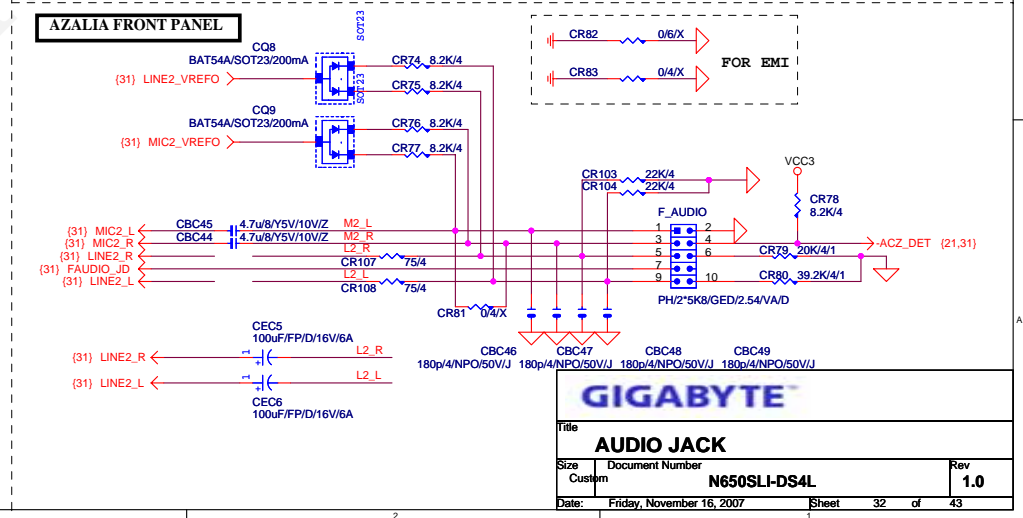
CEN/LFE

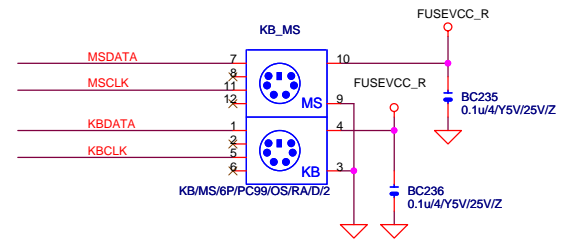
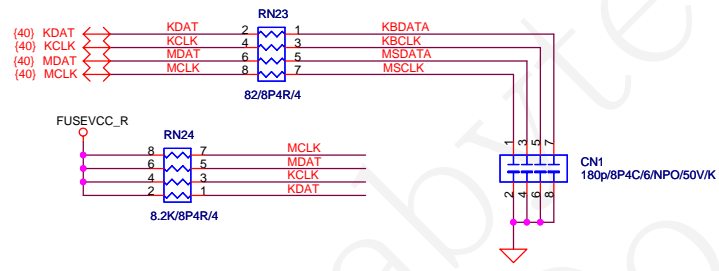
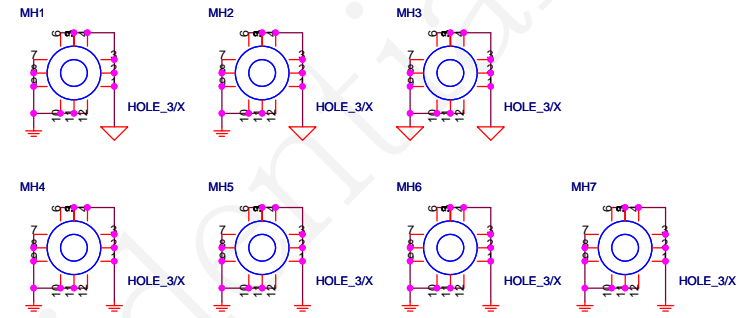


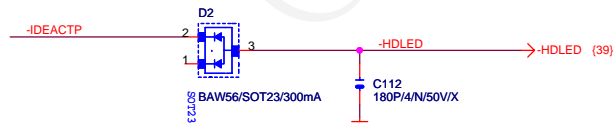
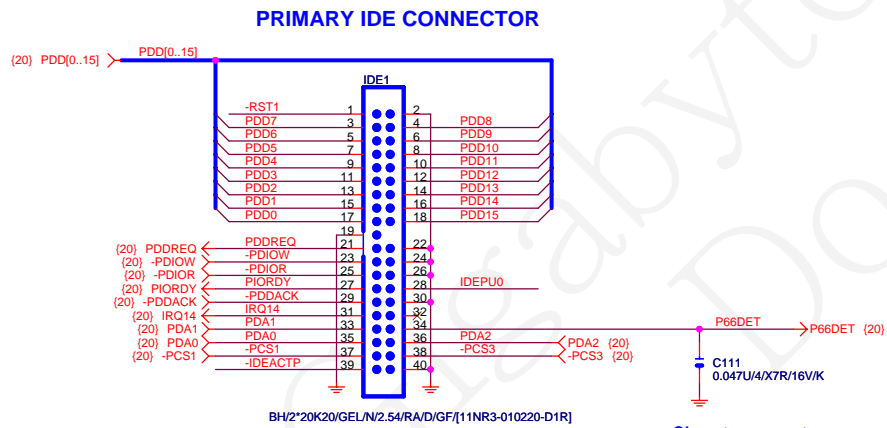
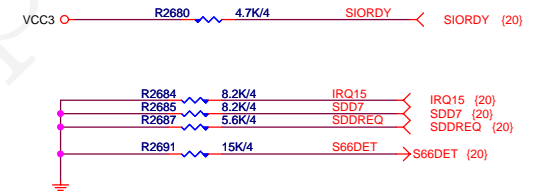
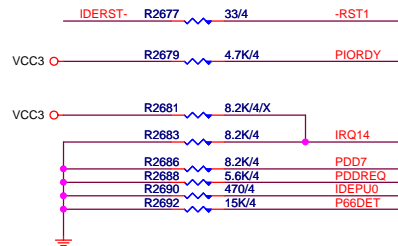
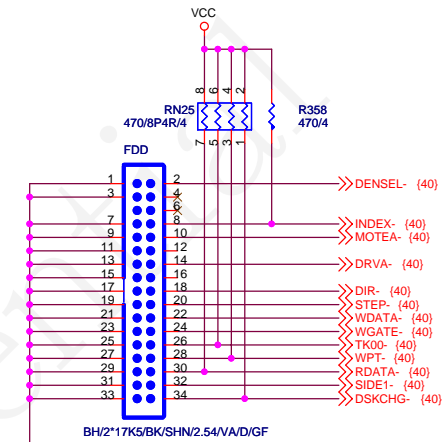
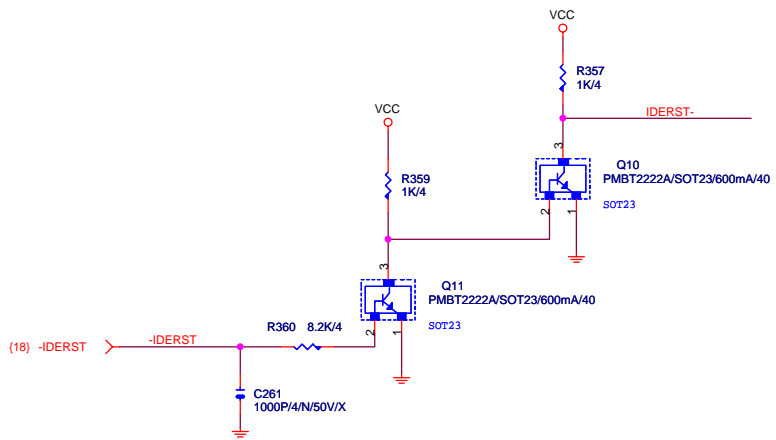
SURR BACK

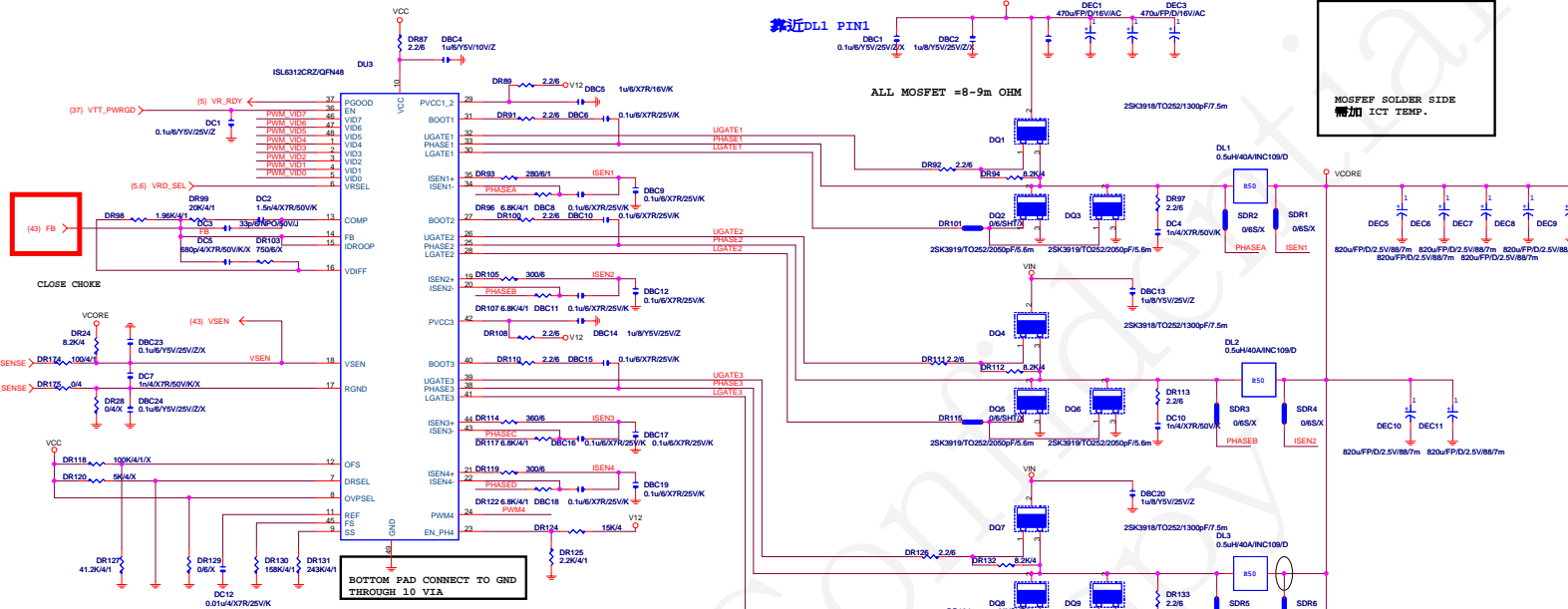


AZALIA FRONT PANEL

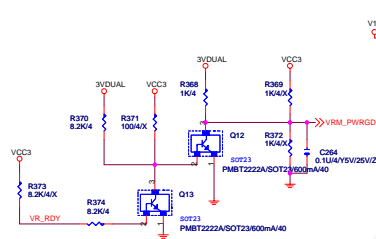






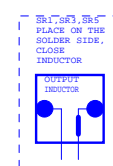
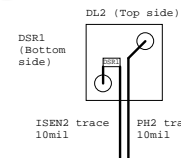
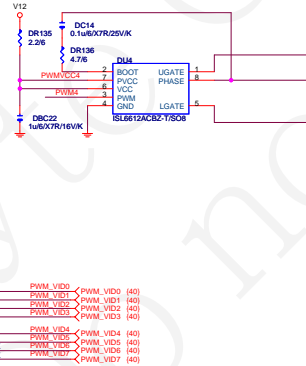
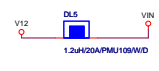
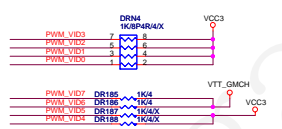


- (21) VORE_OV1 → DR151 8.2K/41 VSEN
- (21) VORE_OV2 → DR152 3.18K/41
- (21) VORE_OV3 → DR153 1.9K/41
- (21) VORE_OV4 → DR154 806/41
- (21) VORE_OV5 → DR155 316/41

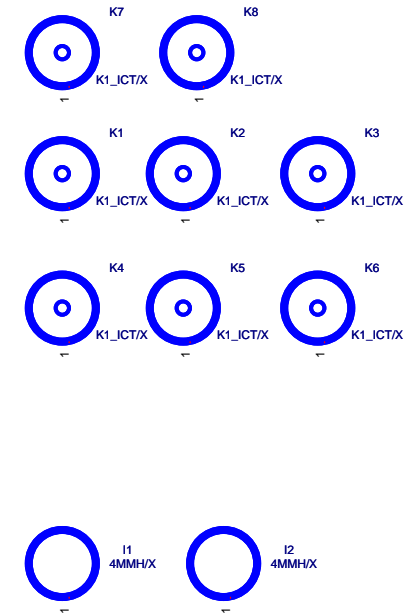
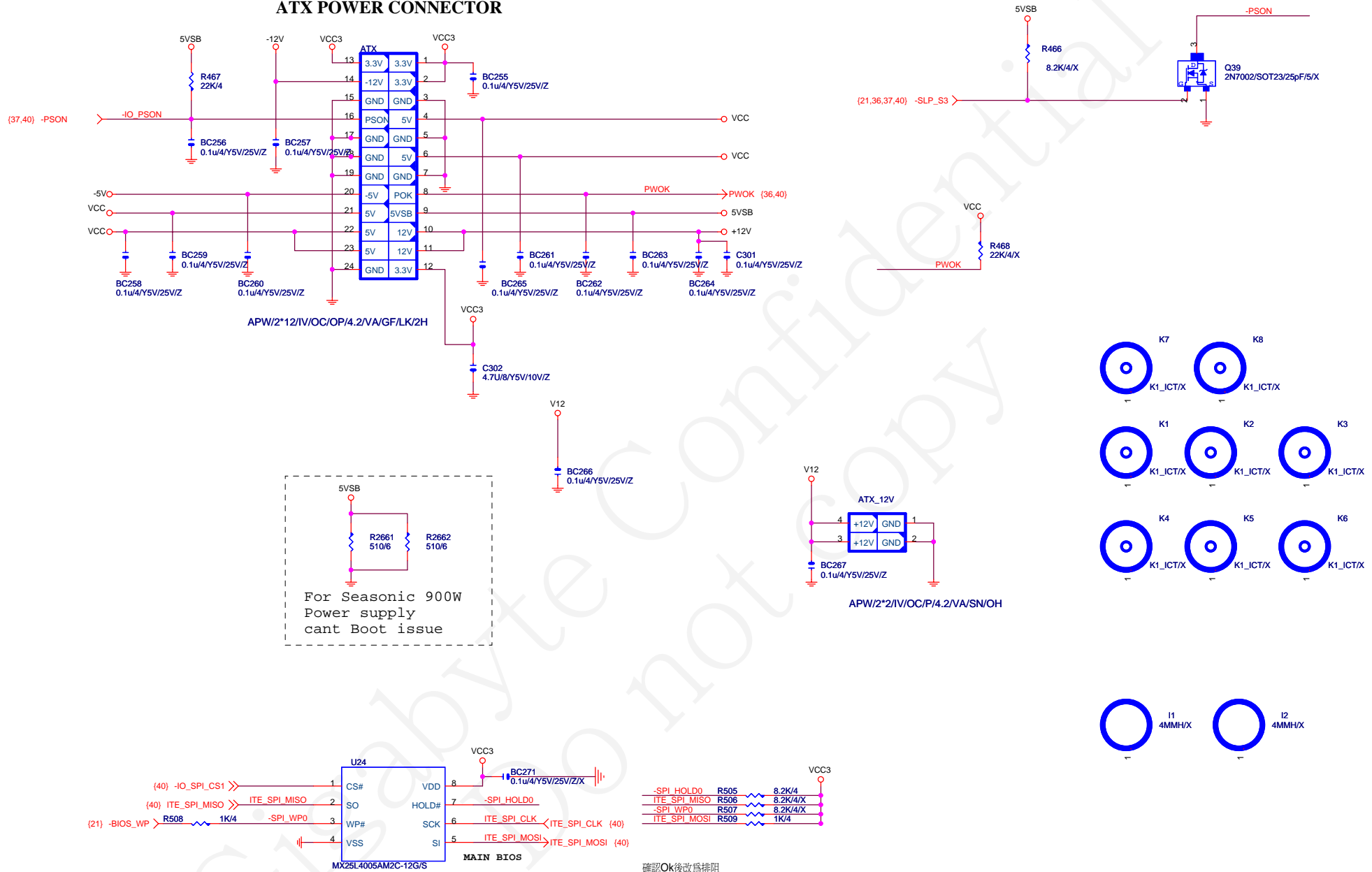


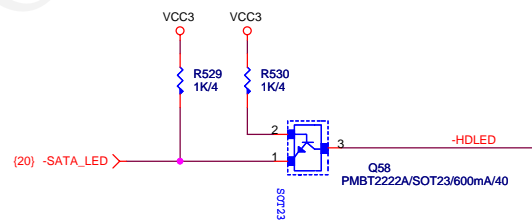
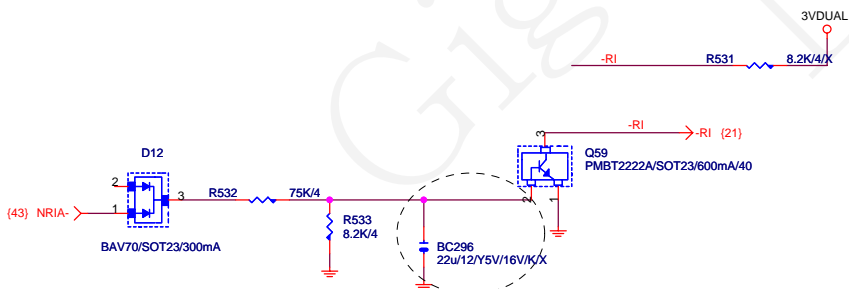
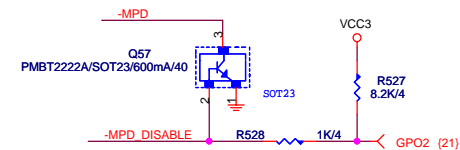
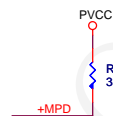
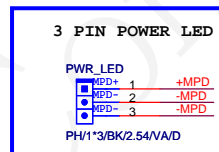
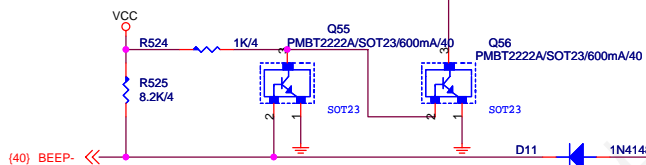
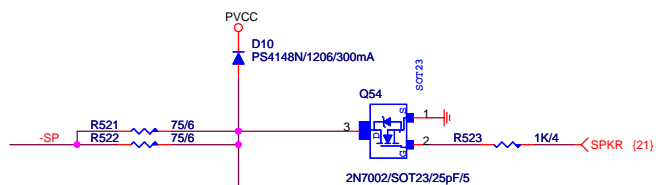
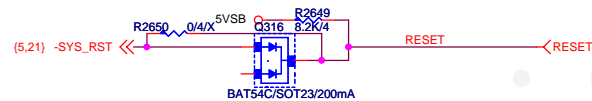
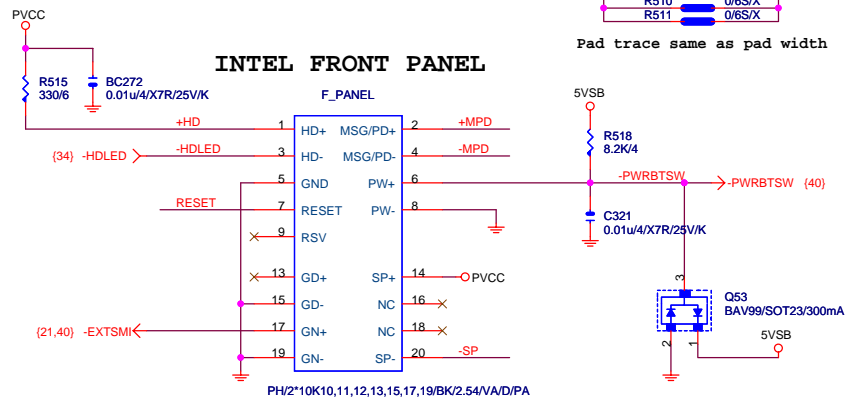
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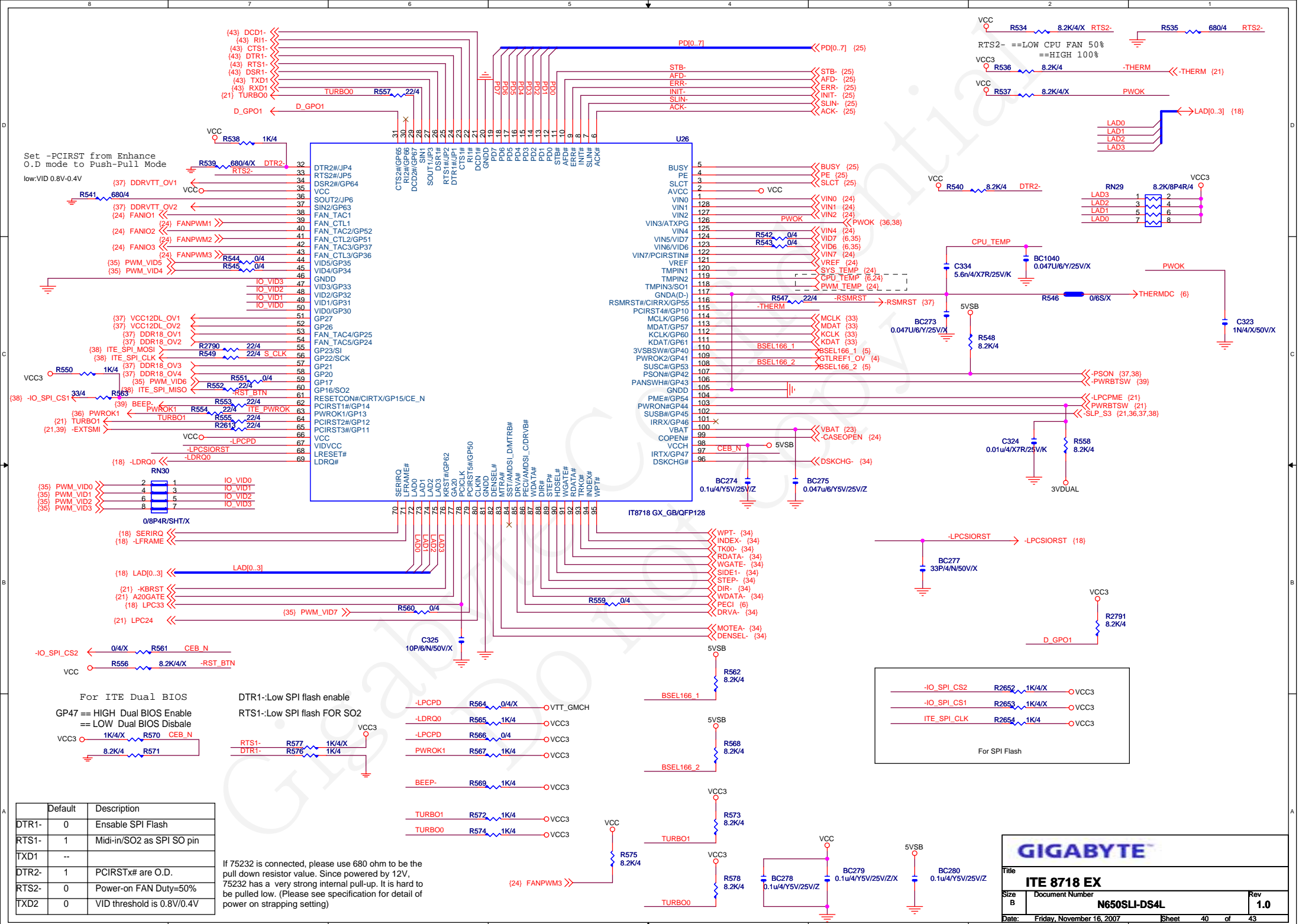
I/O OUTPUT SINK=8mA

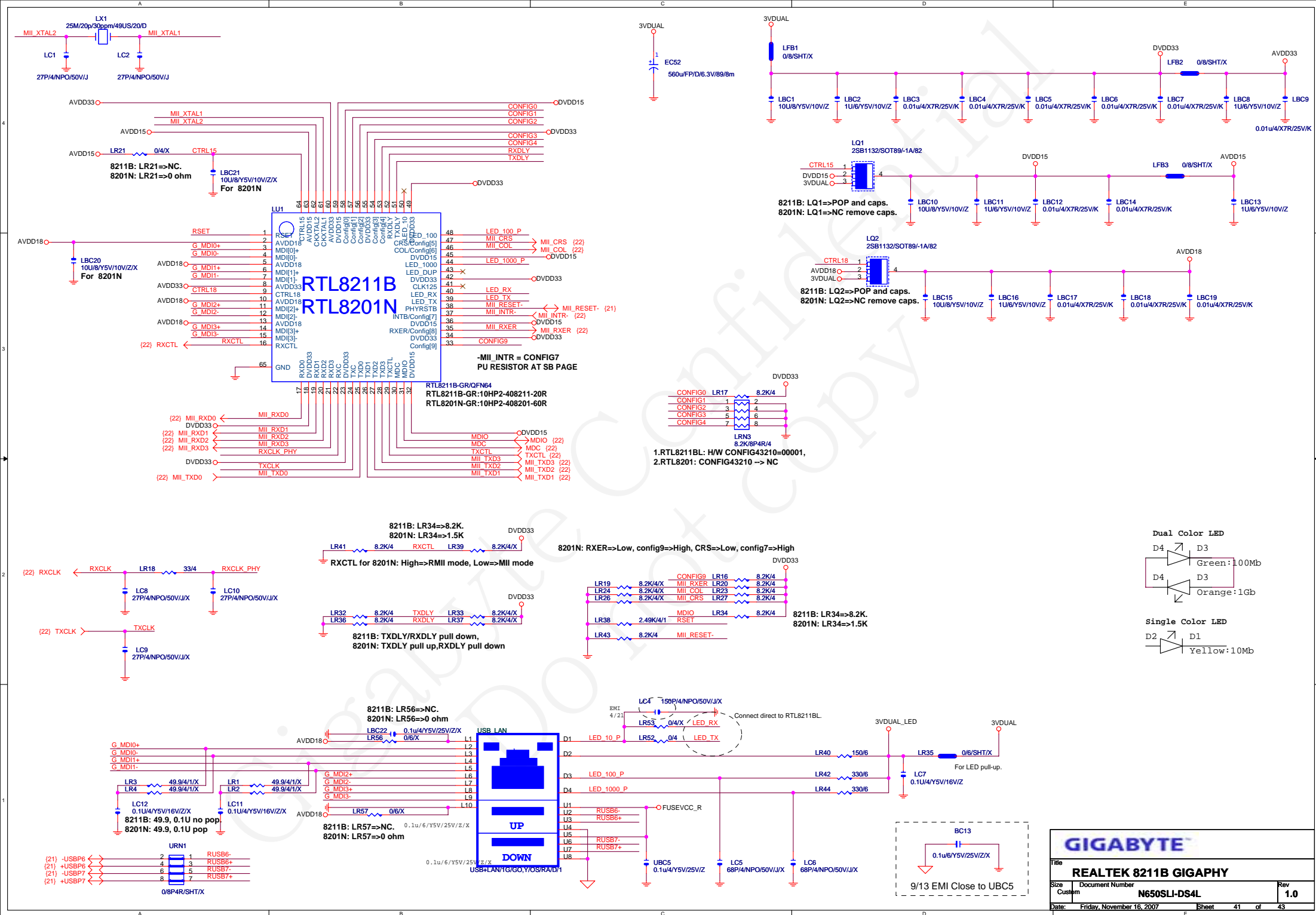


ATX POWER CONNECTOR

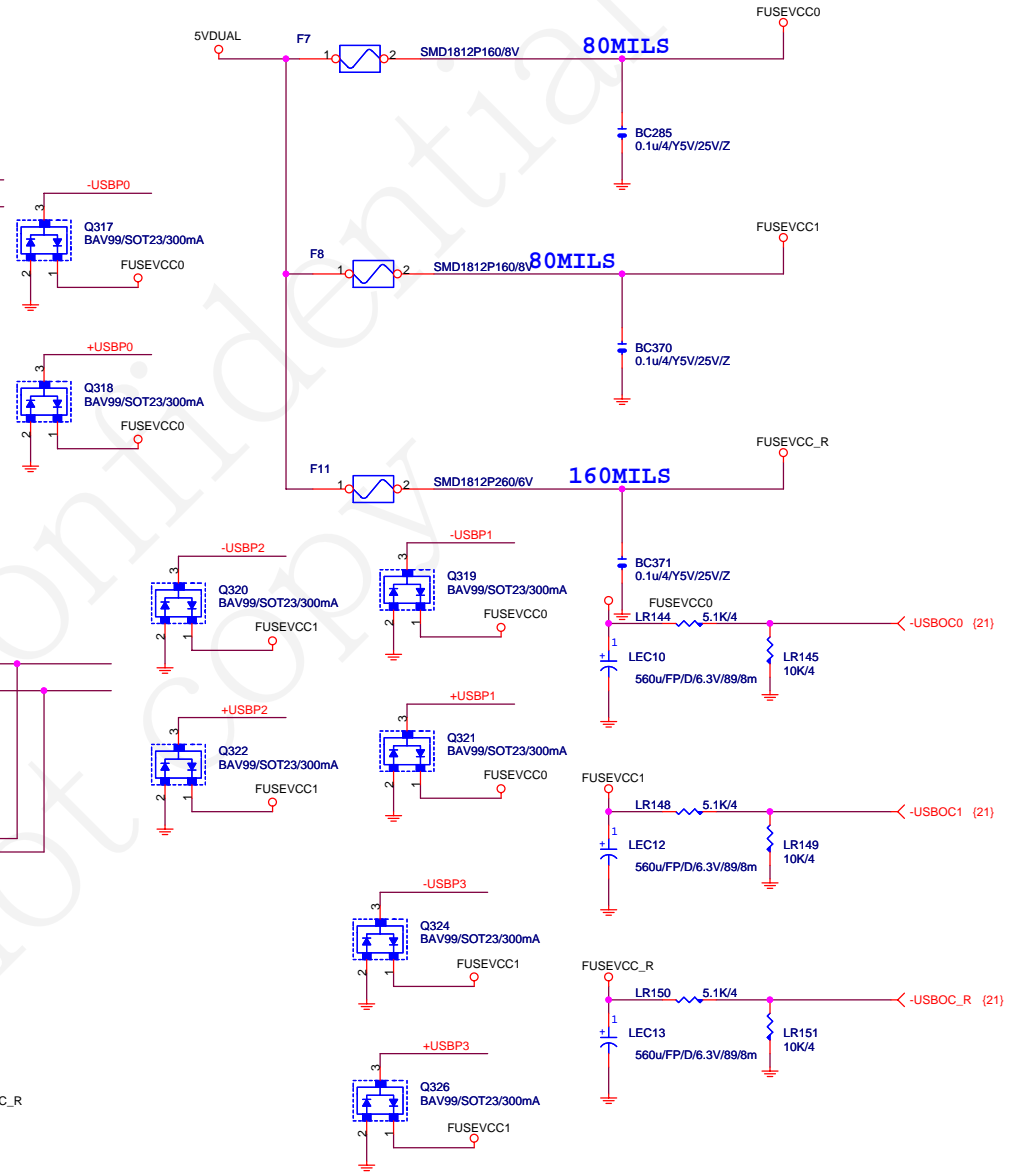
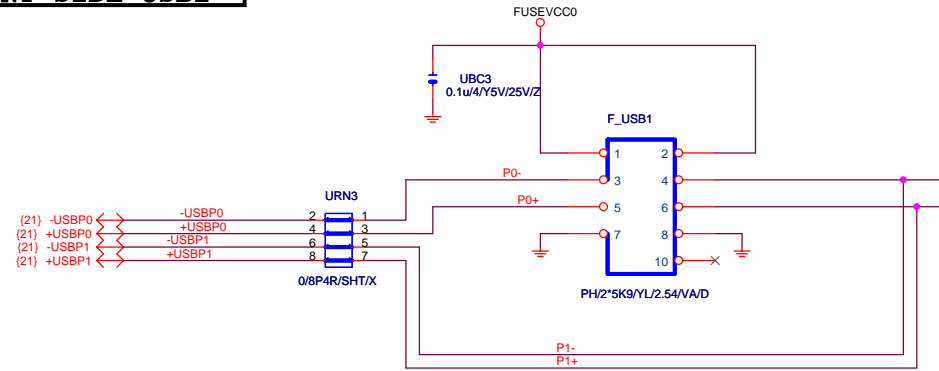








FRONT SIDE USB1



FRONT SIDE USB2

